Tokyo Electron IR Day

January 20, 2021

Forward Looking Statements

- Disclaimer regarding forward-looking statements
  Forward-looking statements with respect to TEL's business plan, prospects and other such information are based on information available at the time of publication. Actual performance and results may differ significantly from the business plan described here due to changes in various external and internal factors, including the economic situation, semiconductor/FPD market conditions, intensification of sales competition, safety and product quality management, intellectual property-related risks, and impacts from COVID-19.
- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.
- Exchange risk
  In principle, export sales of Tokyo Electron's mainstay semiconductor and FPD production equipment are denominated in yen. While some settlements are denominated in dollars, exchange risk is hedged as forward exchange contracts are made individually at the time of booking. Accordingly, the effect of exchange rates on profits is negligible.

FPD: Flat panel display

Agenda

1. Opening 15:30

2. Presentation 15:35
   - Aiming to Enhance the Corporate Value over the Medium to Long Term
   - Supercritical Drying Technology in the Cleaning Process for Leading-edge Devices
   - New Platform for the Etch Systems to Enhance Productivity
   - Latest Single Wafer Deposition Processes and Development Activities for the Future
   - TEL's Strategies toward Digital Transformation

3. Q&A 16:35

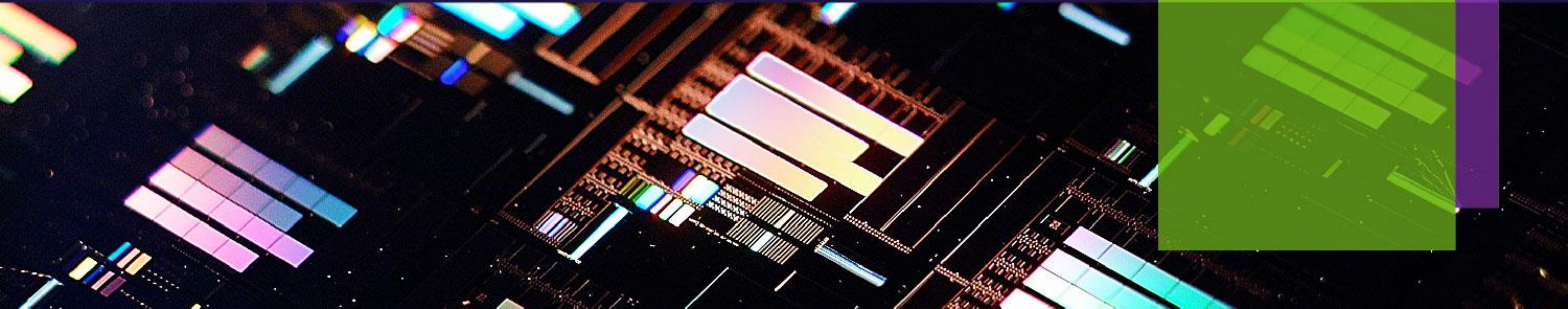
17:15

TOKYO ELECTRON

Aiming to Enhance the Corporate Value over the Medium to Long Term

January 20, 2021

Toshiki Kawai
Representative Director, President & CEO



First and Foremost

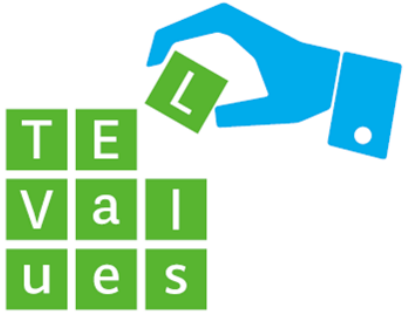
We want to express our deepest sympathies to all those who have been affected by COVID-19 or other natural disasters over the past year

A Year of Steady Progress

TEL's business made steady progress

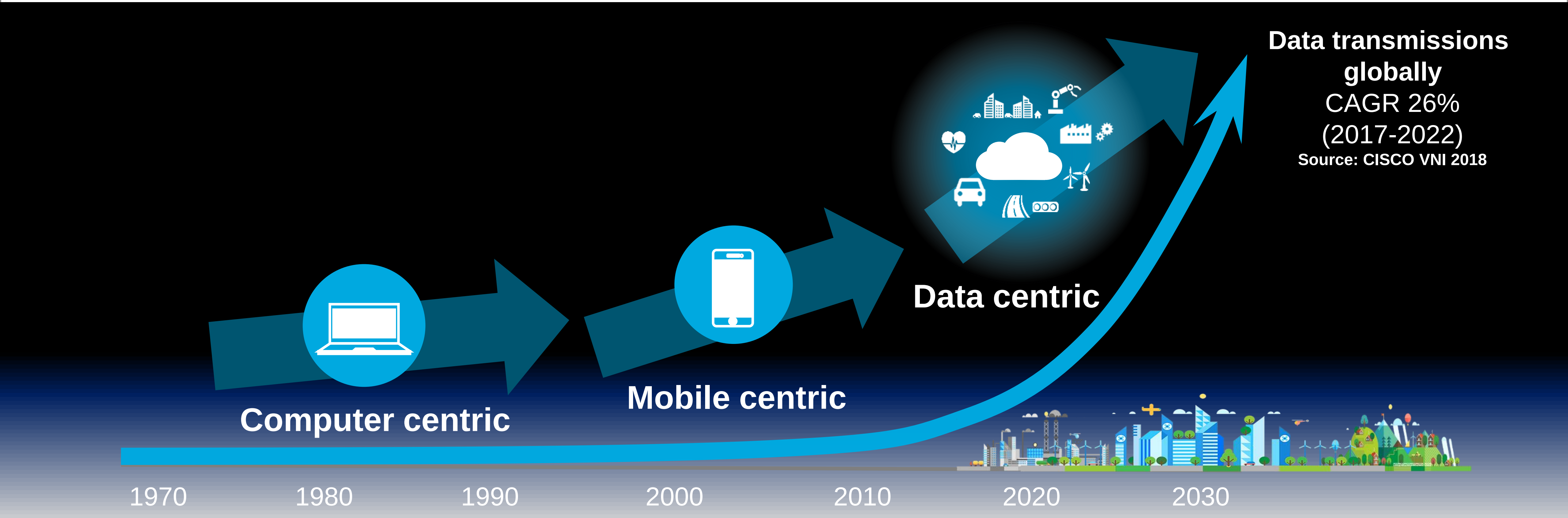
Reaffirmed TEL's driving forces globally

Honored the TEL Values and shared them with employees



Pride・Challenge・Ownership・Teamwork・Awareness

Beginning of Big Data Era



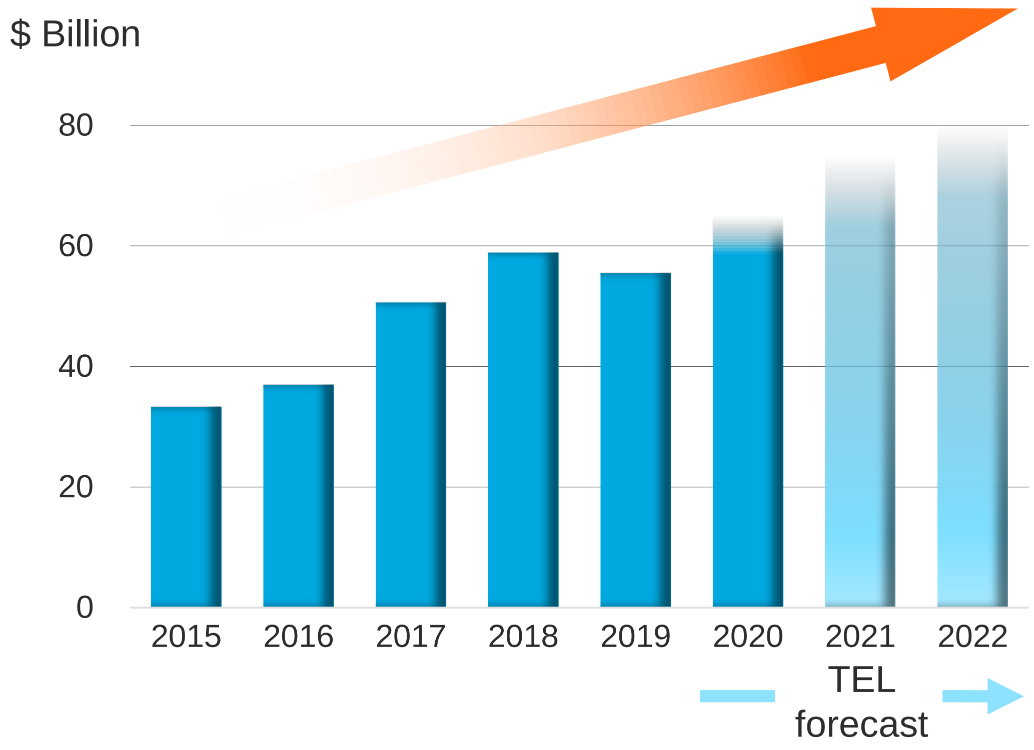
A phase of higher growth with this data-centric era
“Big years” ahead toward a future shift from selling products to selling value

Changes in Society Occurring Amid COVID Crisis

ICT* being implemented widely around the world to build a strong and agile society

* ICT: Information and Communication Technology

WFE* Market



2021:
Increased demand for advanced semiconductors for hyperscale data centers and 5G smartphones will drive WFE market

Memory: Recovery in investment on liquidation of inventories
Logic/Foundry: Continued stable and high level of investment

Last year's record WFE will continue into 2021 and beyond, leading to Big Years

* WFE (Wafer fab equipment): Wafer fab equipment refers to the production equipment used in front-end production and in wafer-level packaging production.

Initiatives to Create New Value Toward Coming Big Years

Tokyo Electron Technology Solutions (TTS)
New production buildings began operation

Tohoku (Iwate): Jul. 2020-

Yamanashi: Aug. 2020-

Enhance production structure to swiftly prepare for future rise in demand

Initiatives to Create New Value Toward Coming Big Years

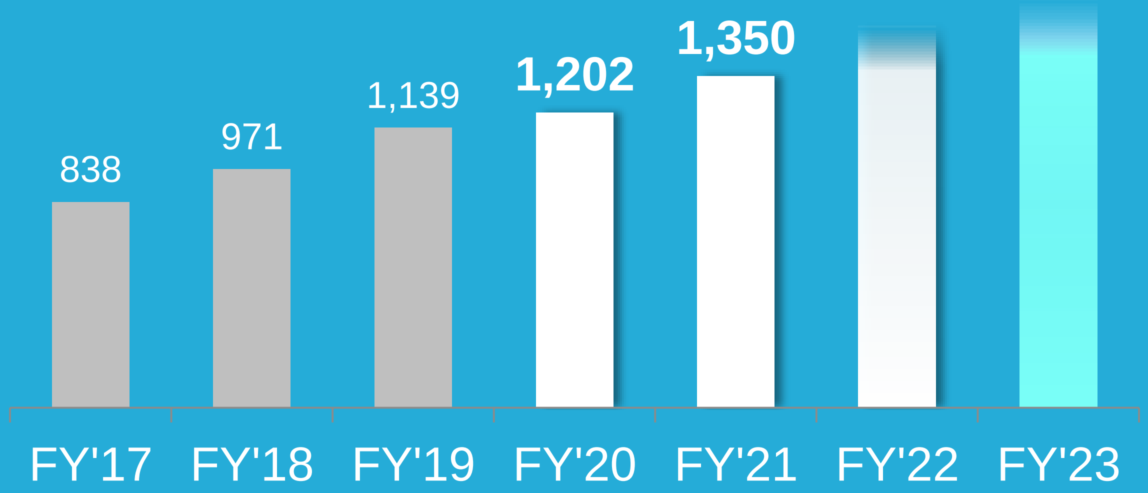
TEL Digital Design Square (Sapporo): Began operation Nov. 2020

Miyagi Technology Innovation Center: Completion scheduled for Sep. 2021

Meet needs for increasingly diverse extreme scaling technology

Initiatives to Create New Value Toward Coming Big Years

¥400B in R&D investment in the three years from FY’20

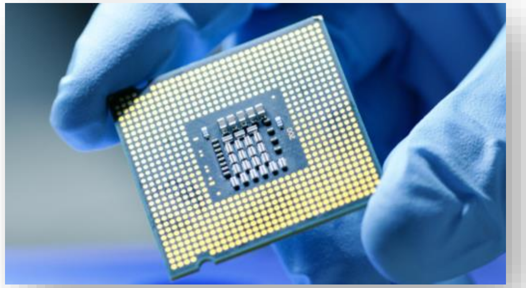


Continue proactive R&D investment to achieve Medium-term Management Plan and maximize capture of growth potential for the future

Initiatives for the Environment

Contribution from business activities

Reduce semiconductor power consumption



SDGs

Tokyo Electron supports the SDGs

Our product initiatives

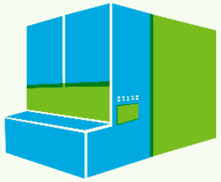
Energy saving, high operation rate and high yield equipment

With our technology both support the development of ICT and reduce environmental burden

Environmental Medium-term Targets for 2030

CO_2 emissions reduction targets

Products



30% reduction

per wafer (**vs 2018**)

Note: Of the total CO_2 emissions from TEL's value chain, approx. 87% are generated during product use

Facilities

70% reduction

of total emissions (vs. 2018)

Reduce energy consumption at each facility by 1% per year (per-unit basis, annual target, YoY)

Toward 100% renewable energy use

Long-term goal (2050)

As a leading corporation in environmental management, Tokyo Electron works actively to conserve the global environment. We strive to contribute to the development of a dream-inspiring society by proactively promoting the reduction of the environmental burden of both our products and facilities, and at the same time, providing evolutionary manufacturing technologies that effectively reduce the power consumption of electronic products.

Support the development of a sustainable society through proactive initiatives for environmental issues

As a SPE and FPD equipment maker

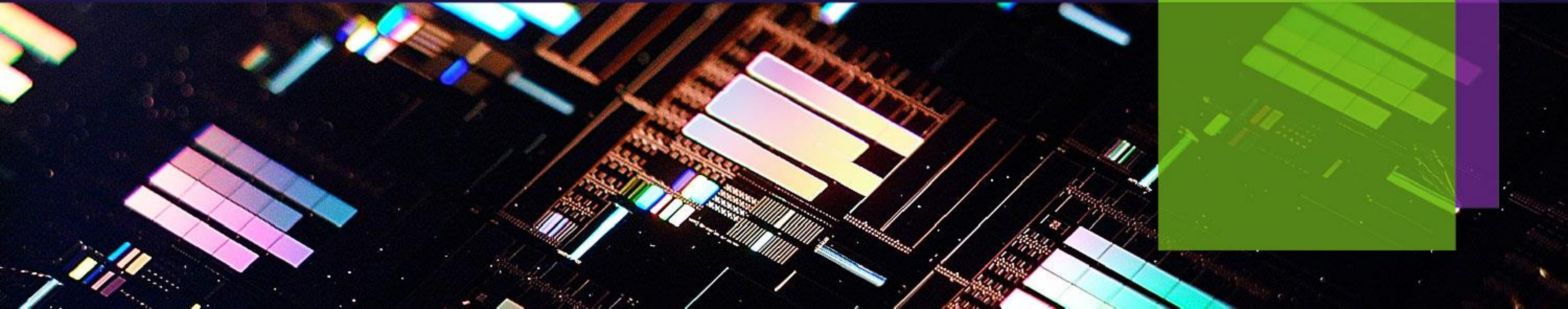
Corporate Philosophy

We strive to contribute to the development of a dream-inspiring society through our leading-edge technologies and reliable service and support.

Supercritical Drying Technology in the Cleaning Process for Leading-edge Devices

January 20, 2021

Keiichi Akiyama
VP & General Manager, CTSPS BU



Release of New Product with Supercritical Drying Technology

TEL Announces the Launch of CELLESTA™ SCD, a Single Wafer Cleaning System

Tokyo Electron (TEL) announced today the launch of the CELLESTA™ SCD single wafer cleaning system, scheduled for release in January 2021.

TEL's CELLESTA series of products are widely used for cleaning silicon wafers in the semiconductor manufacturing process. The soon-to-be-released CELLESTA SCD integrates a dedicated supercritical drying chamber on the mass production-proven CELLESTA platform.

In wafer cleaning, it has been customary to employ low surface tension alcohol solutions in the drying process. However, due to continued semiconductor scaling and adoption of multi-layer structures in highly advanced devices, pattern collapse in the drying process has become one major issue. In response, TEL has developed a pattern collapse-free drying method that uses a supercritical fluid, bringing the technology to the market as equipment for mass production.

With the addition of CELLESTA SCD and its dramatically improved cleaning and drying technologies to the existing line of single wafer cleaning systems, TEL is meeting advanced technological needs in semiconductor manufacturing to drive further growth of the semiconductor industry.

"CELLESTA SCD offers an innovative technological solution to the wafer-drying challenges in the post cleaning process for manufacturing advanced semiconductor devices," said Keiichi Akiyama, Vice President & General Manager, CTSPS BU at TEL. "We will continue to leverage our ability to develop innovative technologies and deliver high value-added products, providing optimum solutions for technological issues associated with the most advanced semiconductor devices."

TEL will be showcasing CELLESTA SCD at SEMICON Japan 2020 Virtual.
Please visit our virtual booth during the show.
Period: 2020/12/11 ～2021/1/15

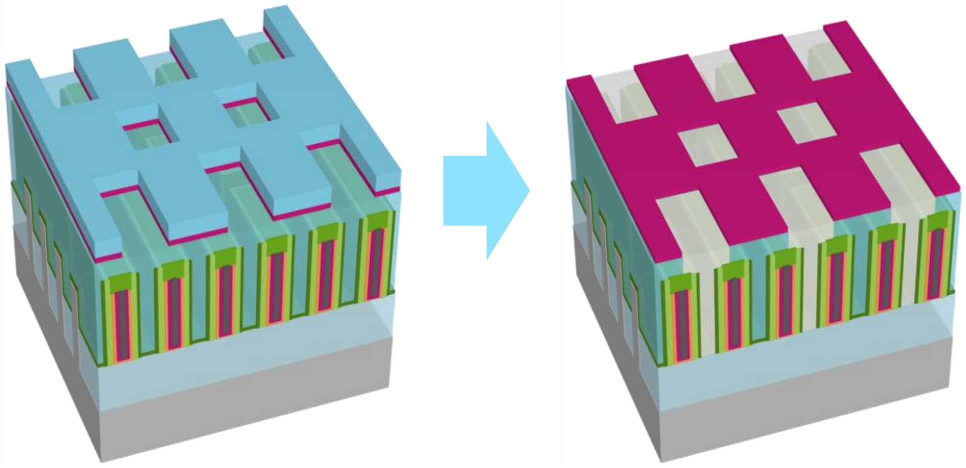
CELLESTA™ SCD

SCD: Supercritical dry

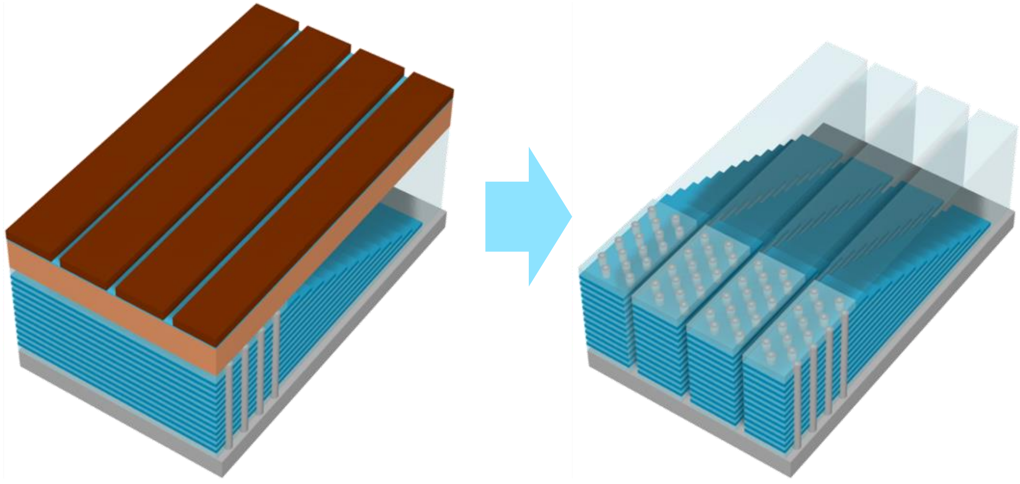
https://www.tel.com/news/topics/2020/20201208_001.html

Cleaning Process in Semiconductor Manufacturing

Post-etch cleaning



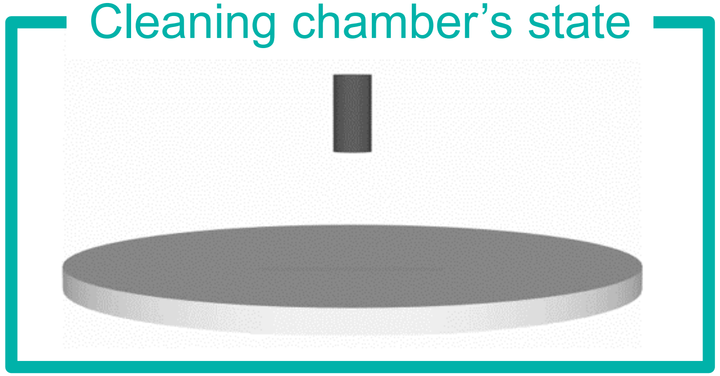
Contact etch



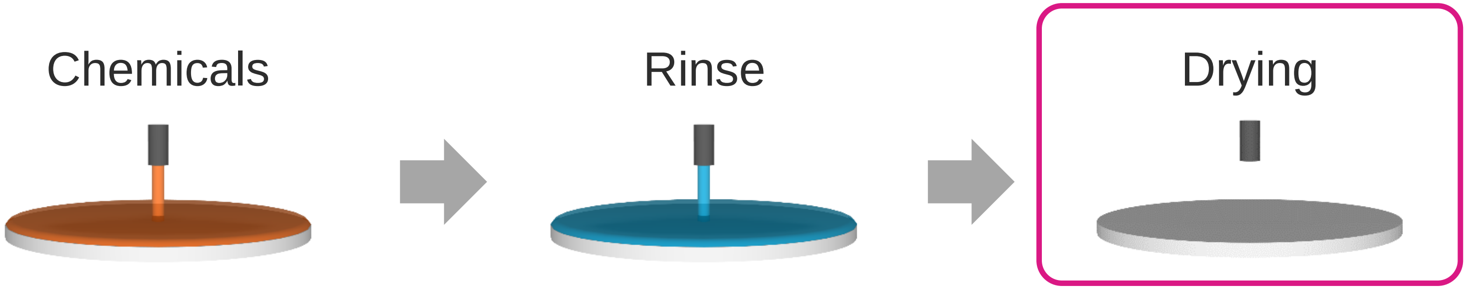
Slit etch

General cleaning process

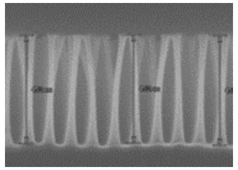
- Cleaning by **chemicals**
- **Rinse**
- **Drying**



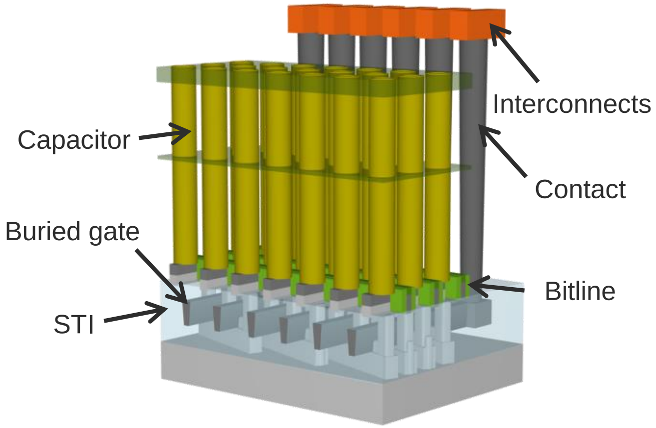
Technology Challenges in Cleaning for State-of-the-Art Devices



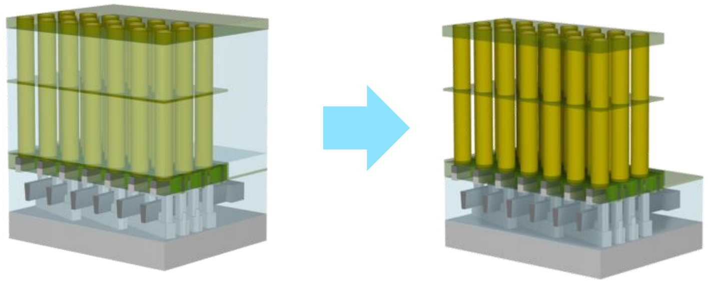
Pattern collapse



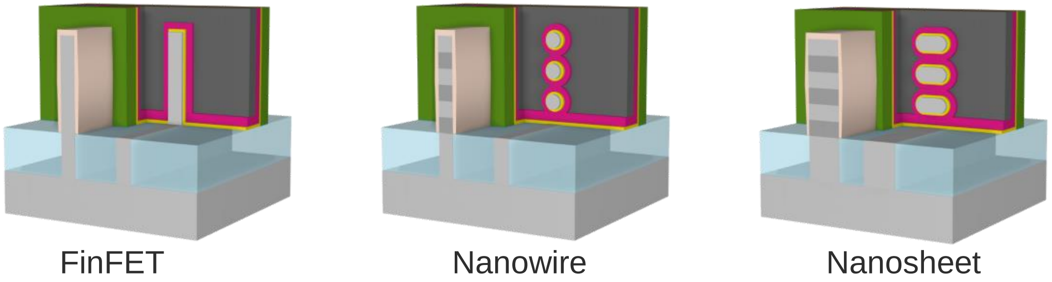
- DRAM
  - Post-STI etch cleaning
  - Mold wet etch after capacitor electrode formation



Wet etch



- Logic
  - Post-fin etch cleaning
  - Post-nanowire/nanosheet formation cleaning



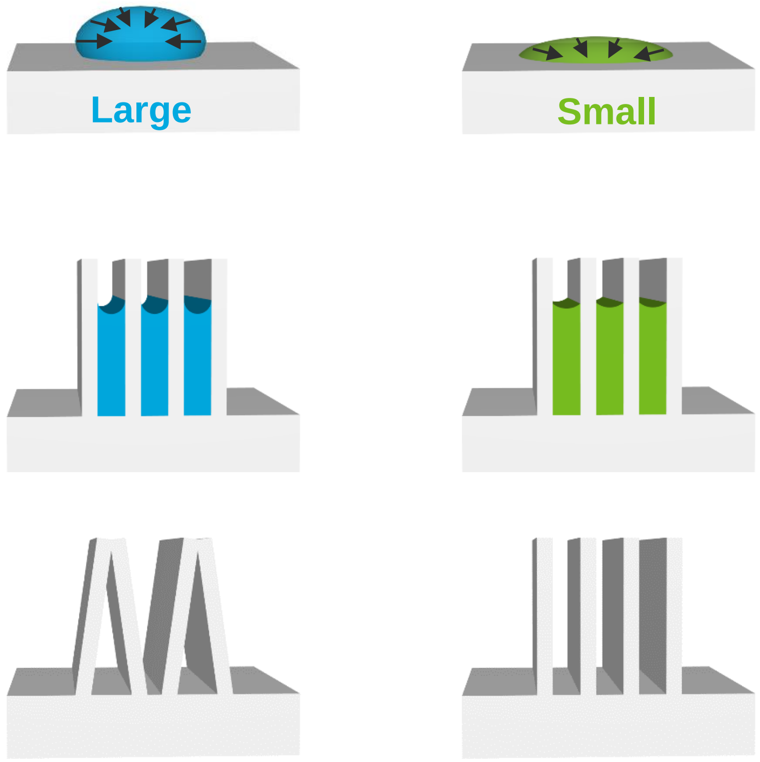
Drying technology more difficult due to further scaling and higher aspect ratios in device manufacturing

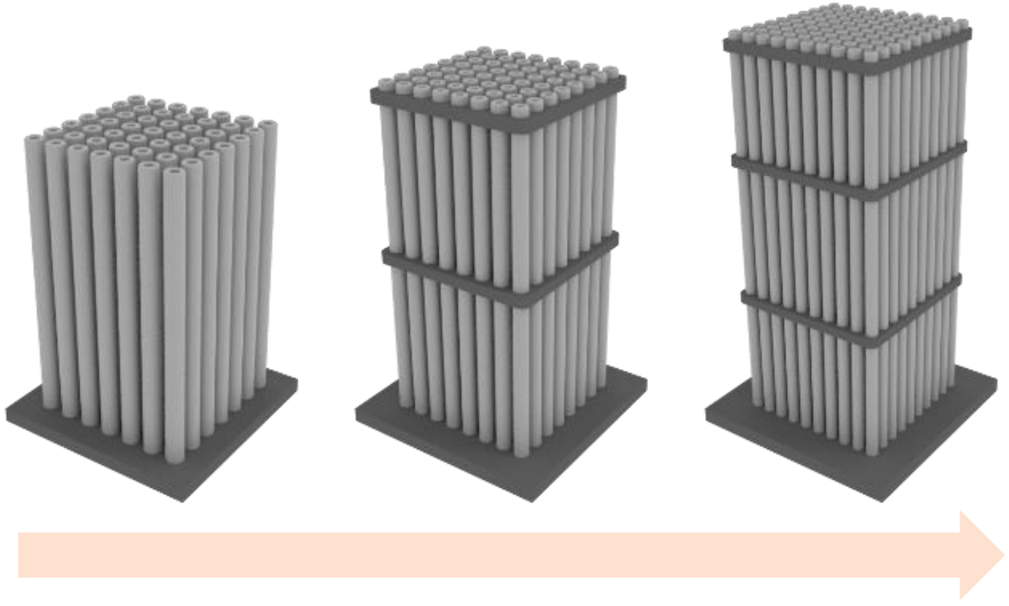
Pattern Collapse Mechanism and Solution

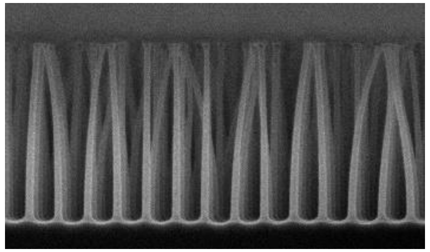
Surface tension*

Before drying

After drying







*Surface tension: The tendency of a liquid or solid to reduce its surface area

As aspect ratios have become higher, the collapse prevention approach of chemical replacement for lowering surface tension, surface modification, etc., is reaching its limit

Next Generation Drying Technology

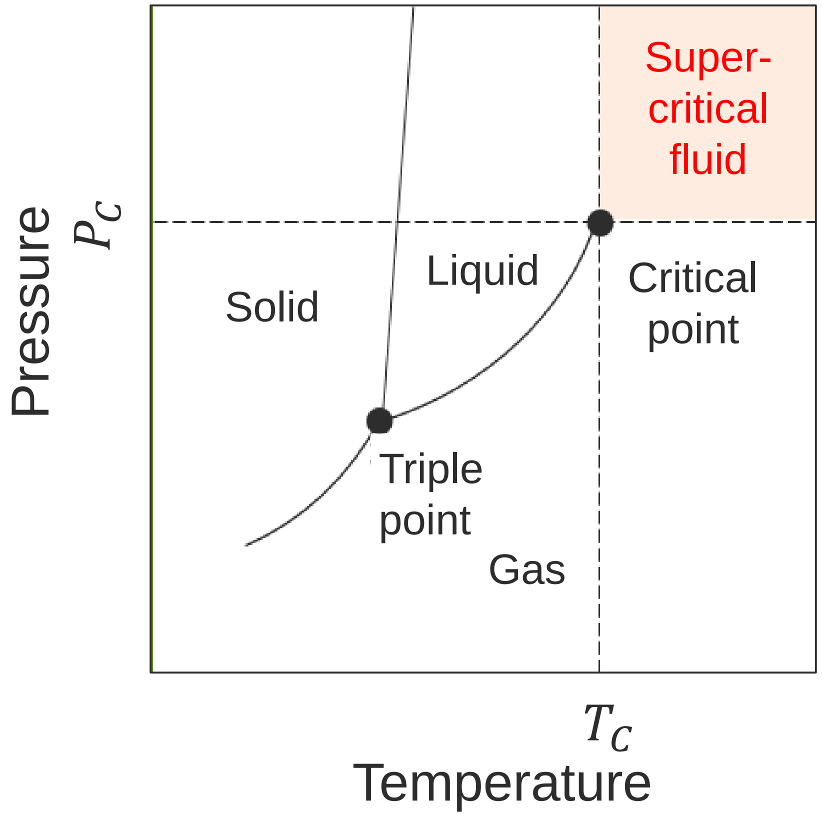
- The next generation drying technologies are supercritical dry and sublimation dry
- As supercritical dry is the most effective solution for the issues in drying technology, TEL has released the CELLESTA™ SCD for mass production
- Supercritical dry is expected to be used in a wide range of applications, including for complex structures like capacitor electrodes and fragile films like PCRAM memory cells

	Application	Residue	Oxidation/material loss
Supercritical dry	Usable for complex and/or high aspect ratio structures	Very little	No
Sublimation dry	Not suitable for stacked or fragile structures	Significant	Yes

Supercritical Drying Technology

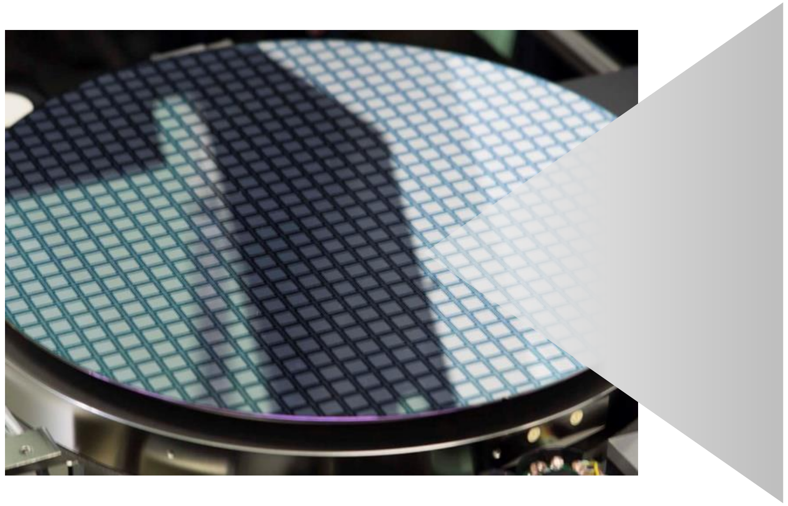
- What is supercritical?
  - The state where temperature and pressure are above their critical point
  - Holds properties between those of liquid and gas
  - Surface tension is zero

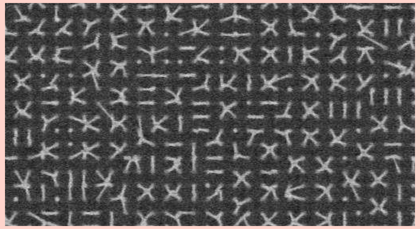
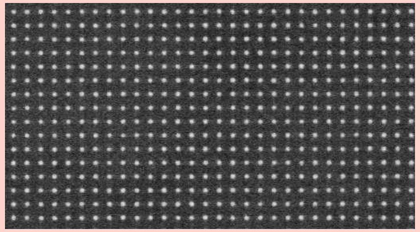
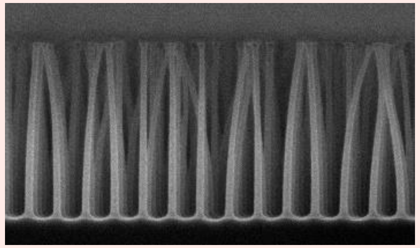
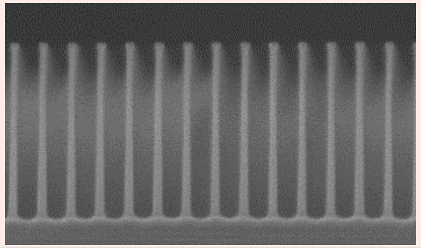
- Challenges for introducing in semiconductor production process
  - Stable operation at pressure regions hitherto unused
  - Particle control at the nano-level



Effective against pattern collapse because surface tension is theoretically zero
Particle control is required at the nano-level for leading-edge processes

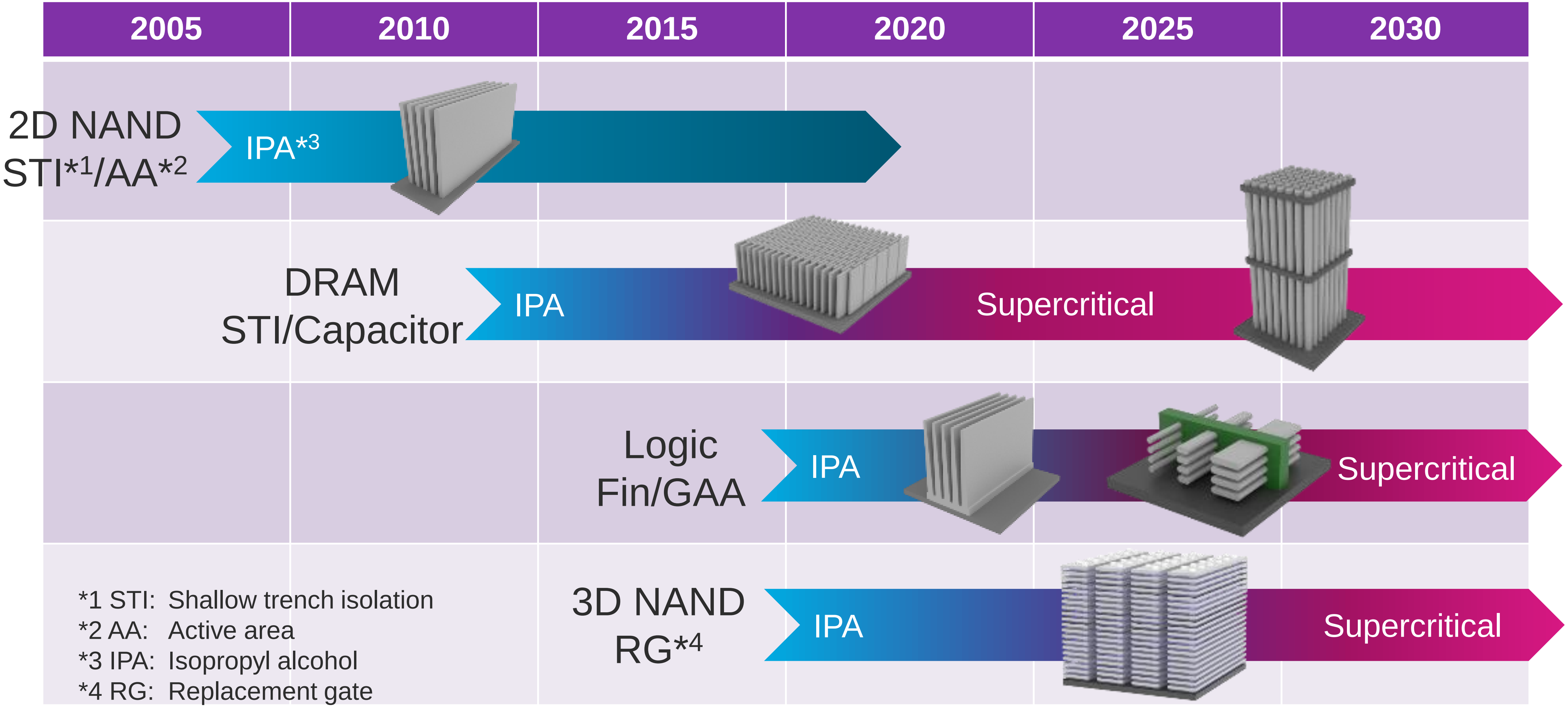
Supercritical Drying Technology



	Traditional drying	TEL's supercritical drying
Top View		
Side View		

Supercritical drying technology prevents pattern collapse

Drying Technology Roadmap



*1 STI: Shallow trench isolation
*2 AA: Active area
*3 IPA: Isopropyl alcohol
*4 RG: Replacement gate

Summary

- TEL is proposing supercritical drying technology for pattern collapse, a technological issue in wafer cleaning

- We will continue to offer new technologies and solutions to various technological issues in wafer cleaning for leading-edge devices as a partner of semiconductor manufacturers

CELLESTA™ Pro SPM

CELLESTA™ -*i*

EXPEDIUS™ -*i*

NS300Z

New Platform for the Etch Systems to Enhance Productivity

January 20, 2021

Isamu Wakui
VP & General Manager, ES BU

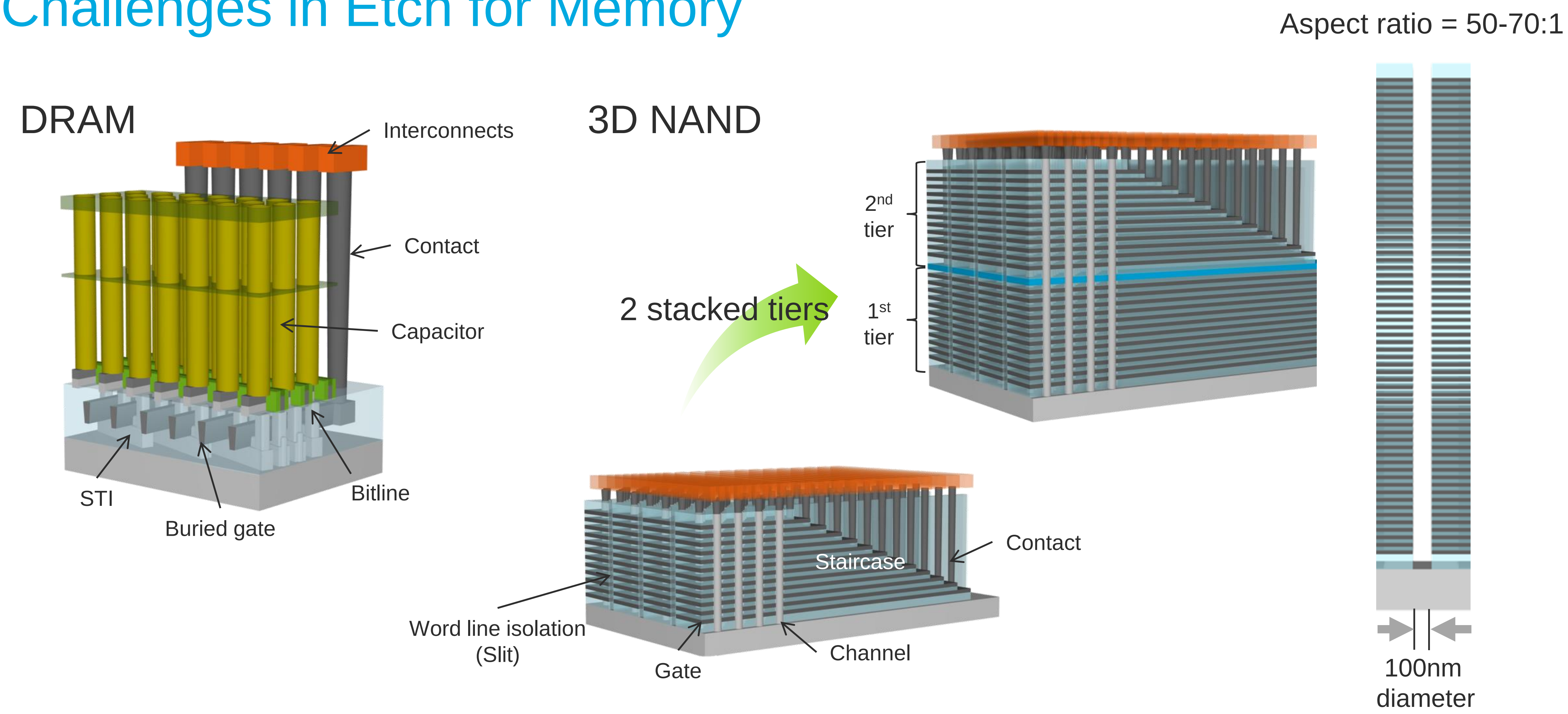
Business Opportunities and Basic Strategy

- Continued high level of investment expected in the etch systems market driven by 3D NAND and patterning

- Focus on HARC, patterning and interconnects, which leverage TEL's strengths
  Aiming to raise share and profitability

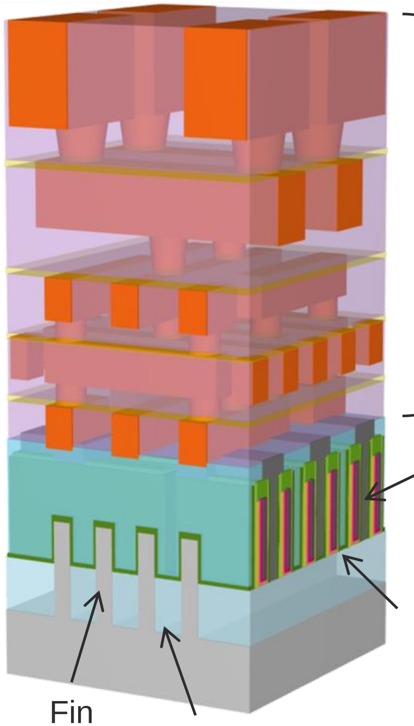
- Continuing proactive investment toward further market growth in future

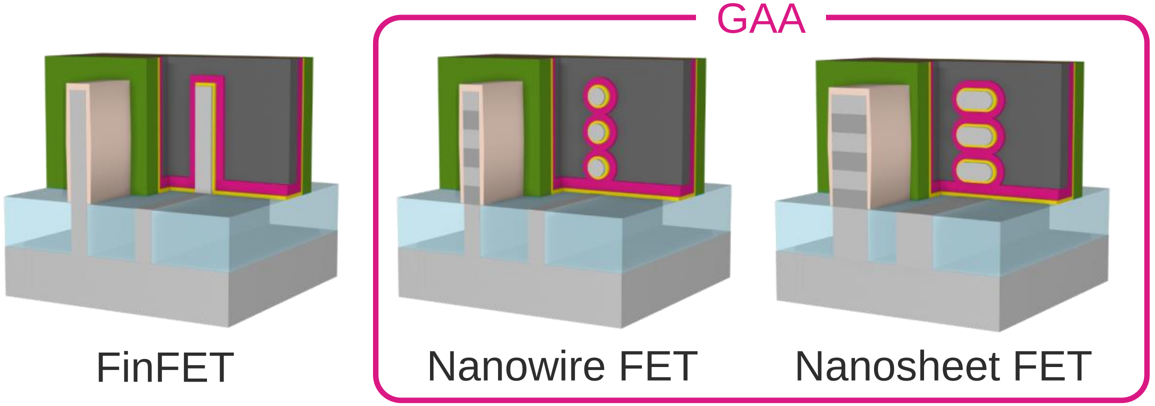
Challenges in Etch for Memory

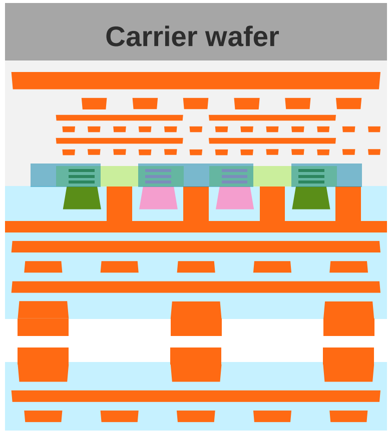


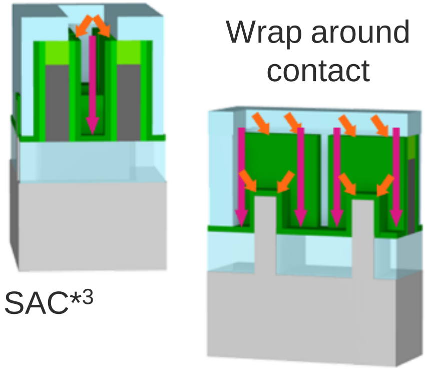
As the number of layers and aspect ratio increase, it is necessary to balance processing performance and productivity

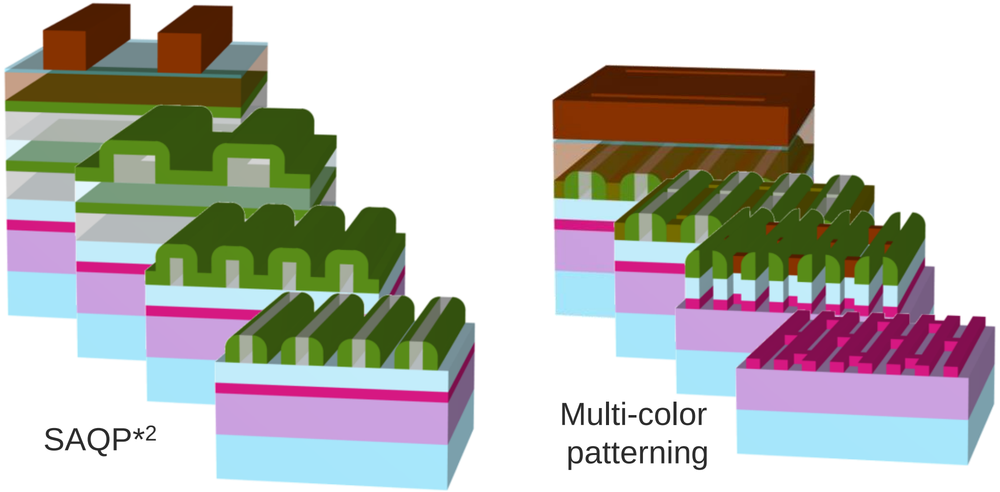
Challenges of Etch for Logic











Flexible equipment layout sought for diversified etch processes

*1 PDN: Power delivery network
*2 SAQP: Self-aligned quadruple patterning
*3 SAC: Self-aligned contact

History of TEL Etch Systems

4, 5, 6 inch | 200 mm | 300 mm

1980's | 1990's | 2000's | 2010's

TEL Etch 480
TEL's first single wafer dry etch tool

UNITY™
TEL's first original vacuum multi-chamber tool

Telius™
World's first parallel-chamber tool

Tactras™
World's first addition of X axis movement to robot arm
Realized 6 chambers in one system

TE5000
TEL's first original dry etch tool

TE8500

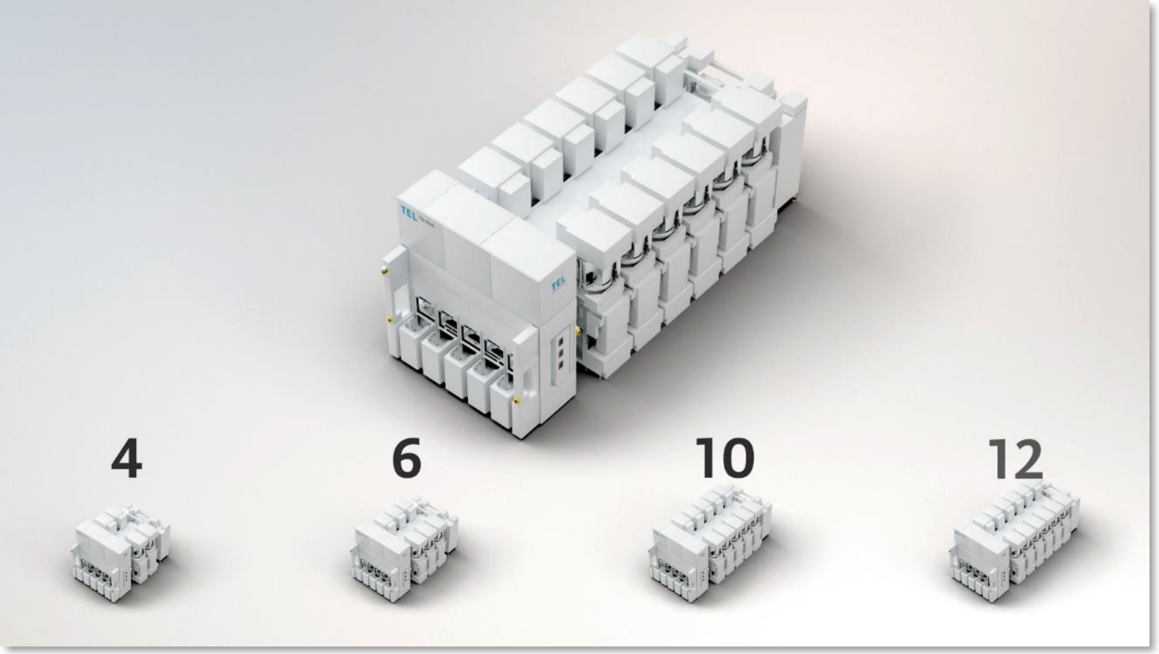
UNITY™ II
TEL's first platform with multi-chambers

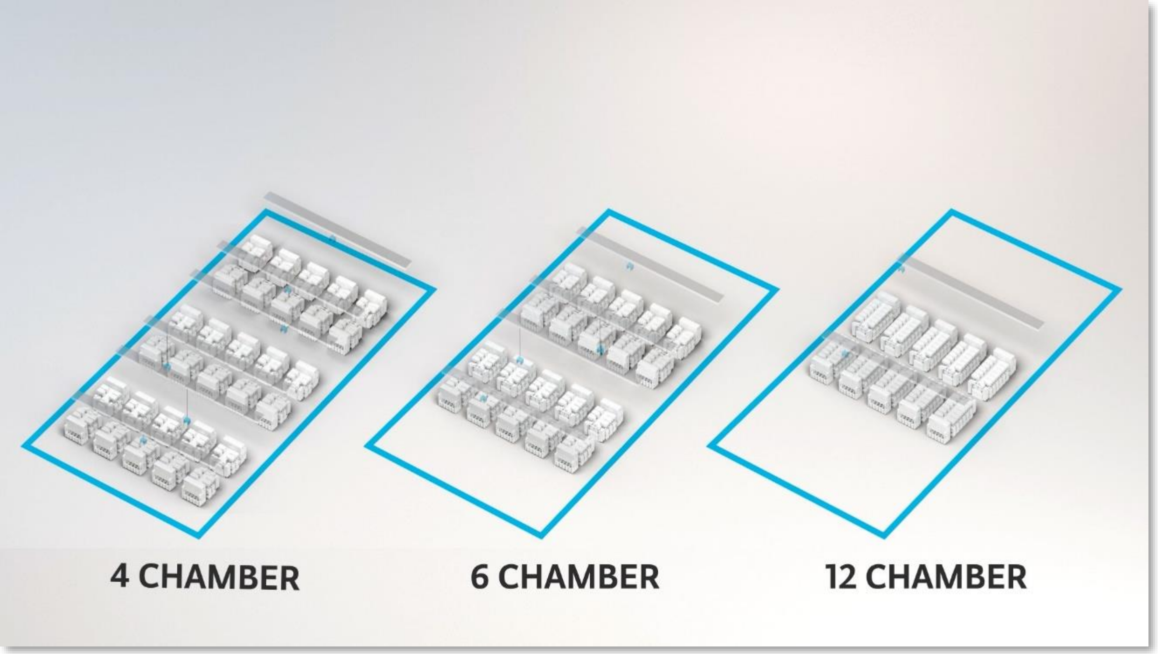
Tactras™ BX
Realized 8 chambers in one system

Episode™ UL Features

Flexible layout available to accommodate needs
Improved productivity through space saving and smart tools

Episode™ UL: Layout

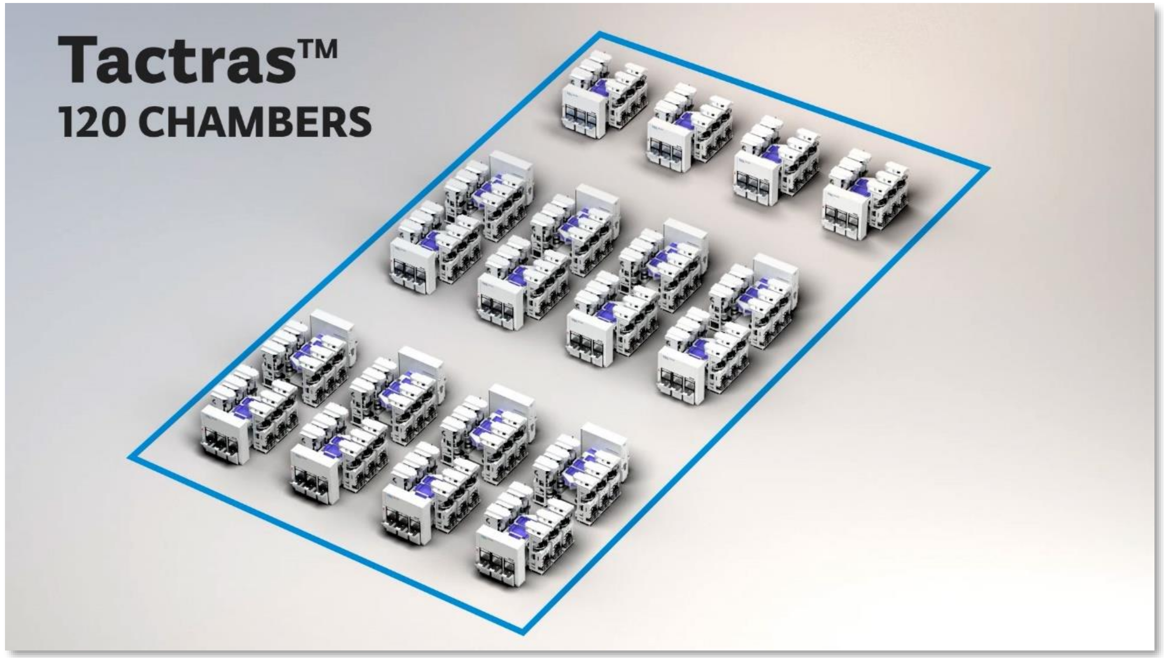


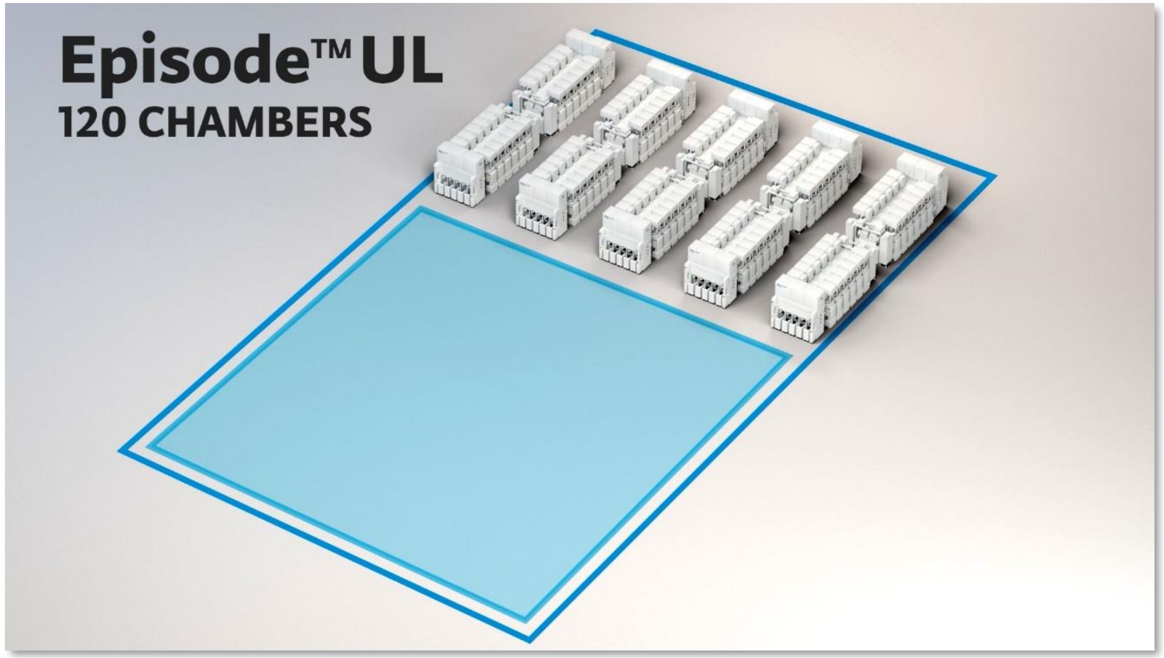


Select from 4 options
4, 6, 10, and 12 chamber designs

Flexible layout available to accommodate
fab space and target processes

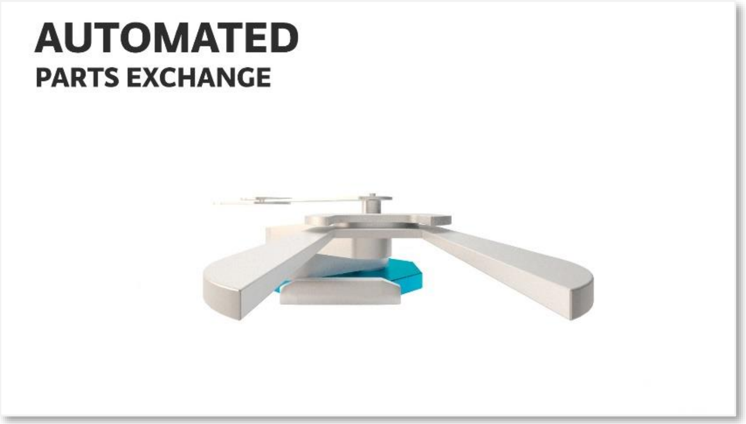
Episode™ UL: Space





Significantly reduced footprint per chamber

Episode™ UL: Smart Tools



Includes automated parts exchange functions, multiple sensors and a high-speed control system
Autonomous process control possible through big data analysis using TEL's own smart tools

Episode™ UL Movie

Summary

- Flexible layout:
  - Capable of selecting any number of chambers, from 4 to 12

- Space:
  - Significantly reduced footprint per chamber

- Smart Tools:
  - Includes automated parts exchange functions, multiple sensors and a high-speed control system

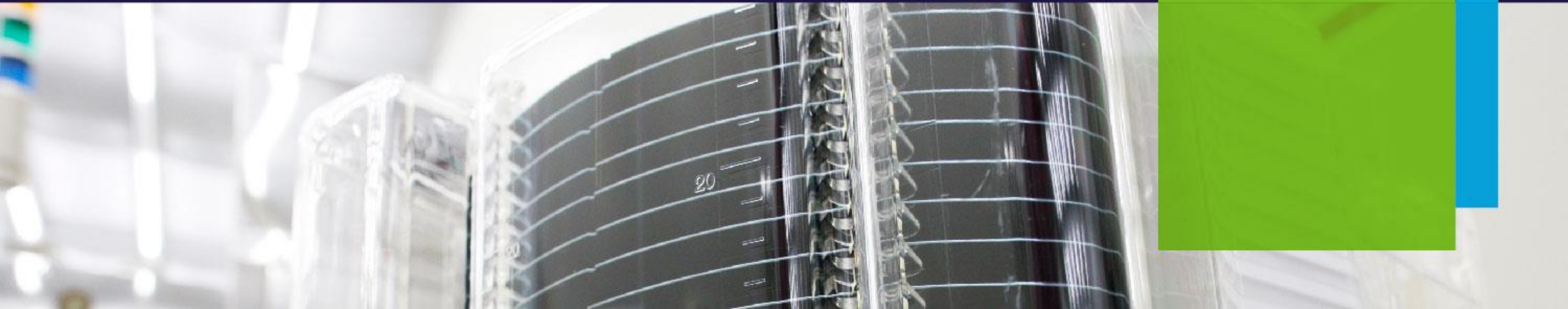
  Autonomous process control possible through big data analysis using TEL's own smart tools

TOKYO ELECTRON

Latest Single Wafer Deposition Processes and Development Activities for the Future

January 20, 2021

Hiroshi Ishida
VP & General Manager, TFF BU



Thin Film Formation Product Lineup

Furnace
TELINDY PLUS™

Semi-batch ALD
NT333™

Single Wafer Deposition
Triase+™

MRAM MTJ Formation
EXIM™

Oxidation / CVD / ALD / PVD

Batch Process*

Process: Oxidation/CVD/ALD
Reaction: Thermal/Plasma
Material: SiO_2/Si_3N_4/High-k/Metal
Feature: 100 to 150 wafers/batch

Semi-batch Process

Process: ALD
Reaction: Thermal/Plasma
Material: SiO_2/Si_3N_4/High-k
Feature: 5 to 6 wafers/batch

Single Wafer Process

Process: CVD
Reaction: Thermal/Plasma
Material: Metal/High-k/Ferroelectric
Feature: Superior step coverage

Process: PVD
Reaction: Thermal/Plasma
Material: Magnetic material/Metal
Feature: Multi-film stacking

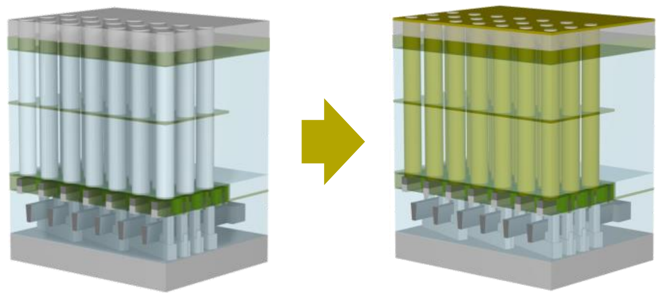
* Installed base >10,000 @ 300mm

Triase+™ EX-II™ Advance: TiN for Super High Aspect Ratio

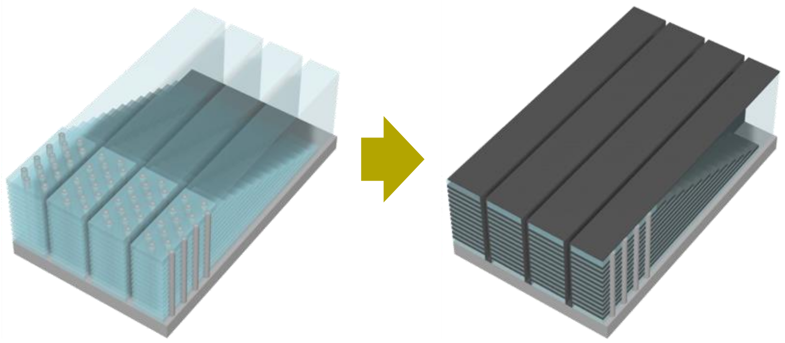
- Features
  - State-of-the-art advanced sequential flow deposition (TiN)
  - High precursor and gas supply provides superior step coverage ratio for the most advanced memory devices
  - Thin film continuity (Continuous film at <10 Å)
  - Excellent thickness uniformity (1σ < 1%)
  - Wide temperature capability (400 to 600℃)
  - High speed pressure control enables higher productivity

- Applications
  - DRAM capacitor electrode
  - 3D NAND word line barrier
  - Other high surface area structures

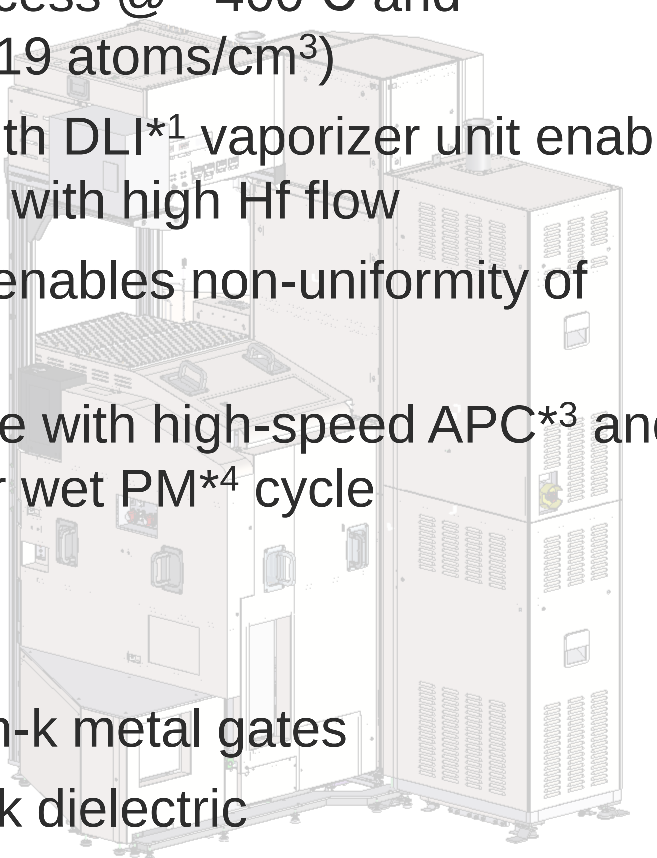
DRAM Bottom electrode



3D NAND Word liner barrier



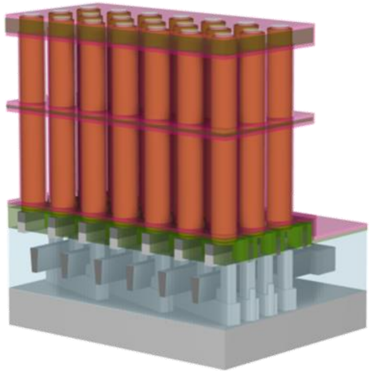
Triase+™ EX-II™ HK: High Quality High-k Dielectric



- Features
  - Designed for HfO process @ ~400°C and ultra low carbon (~1E19 atoms/cm^3)
  - Liquid Hf precursor with DLI*1 vaporizer unit enables ideal ASFD*2 process with high Hf flow
  - Unique gas insertion enables non-uniformity of < 1% within wafer
  - Enhanced exhaust line with high-speed APC*3 and 100A piping for longer wet PM*4 cycle
- Applications
  - DRAM peripheral high-k metal gates
  - 3D NAND block high-k dielectric

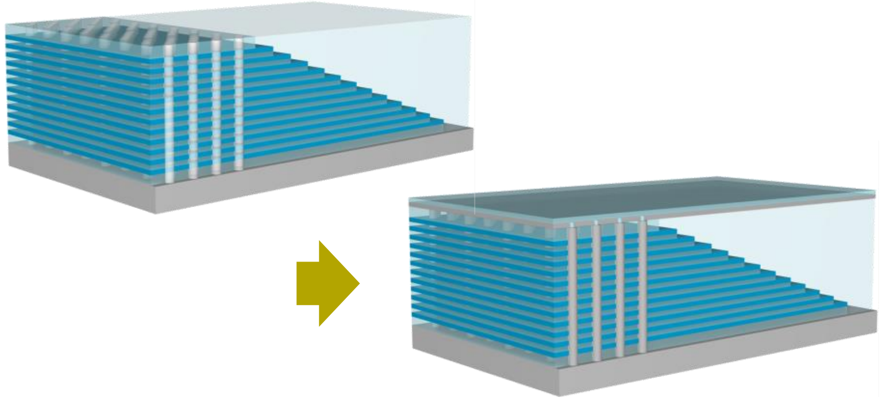
DRAM

High-k dielectric



3D NAND

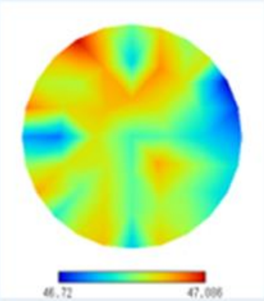
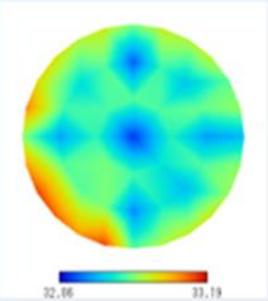
Block high-k ~ core oxide dep



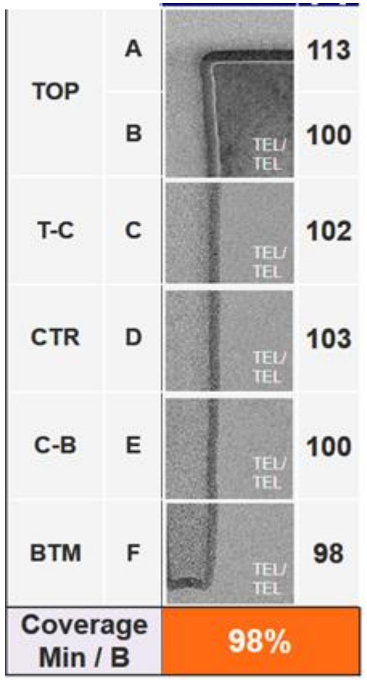
*1 DLI: Direct liquid injection
*2 ASFD: Advanced sequential flow deposition
*3 APC: Auto pressure control valve
*4 PM: Preventative maintenance

Triase+™ EX-II™ HK: High Quality High-k Dielectric

Uniformity

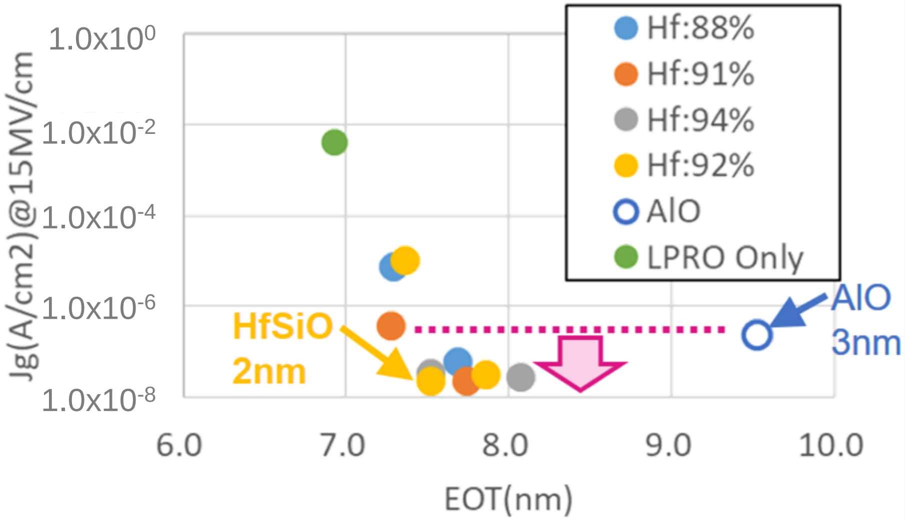
	HfSiO	HfO
Hf conc. (%)	73	100
Map		
Ave. thick (Å)	46.9	33.0
Range (%)	0.78	0.85
1σ (%)	0.16	0.19
Ave. - IL	32.0	19.9

Coverage



Hole aspect ratio = 55:1

Leak current



Leak current of HfSiO 2nm-thick is smaller than that of AlO 3nm-thick on TEL MOS capacitor

Enables high-k thin film formation on high aspect ratio structures

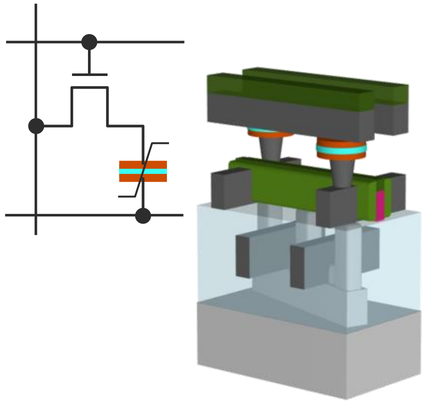
Triase+™ EX-II™ MS: Multi-source Supply for Controllable Film Composition

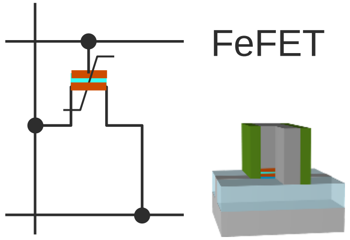
Under development

- Features
  - New Chamber design for multi-source supply
  - Capable of composition ratio control

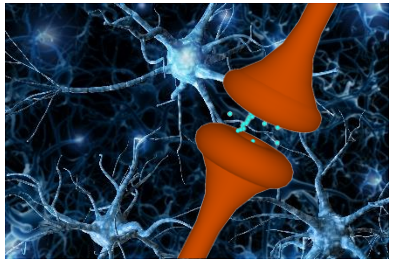
- Applications
  - Ferroelectric FET for non-volatile memory
  - Extension to storage class memory
  - Extension to neuromorphic devices (memorizing synaptic weight)

FeRAM

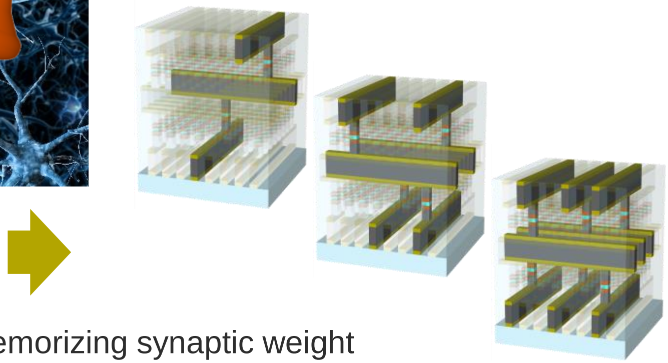




Neuromorphic



Artificial synapse

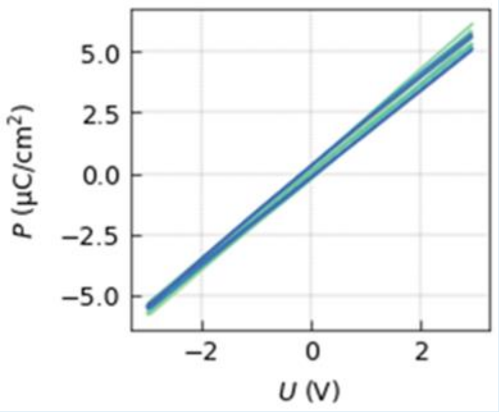
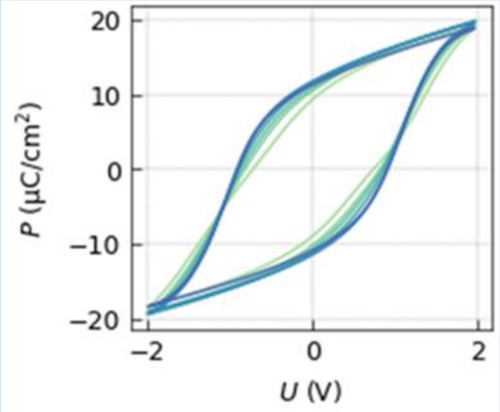
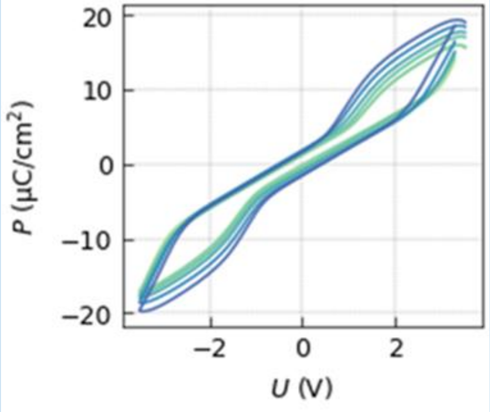


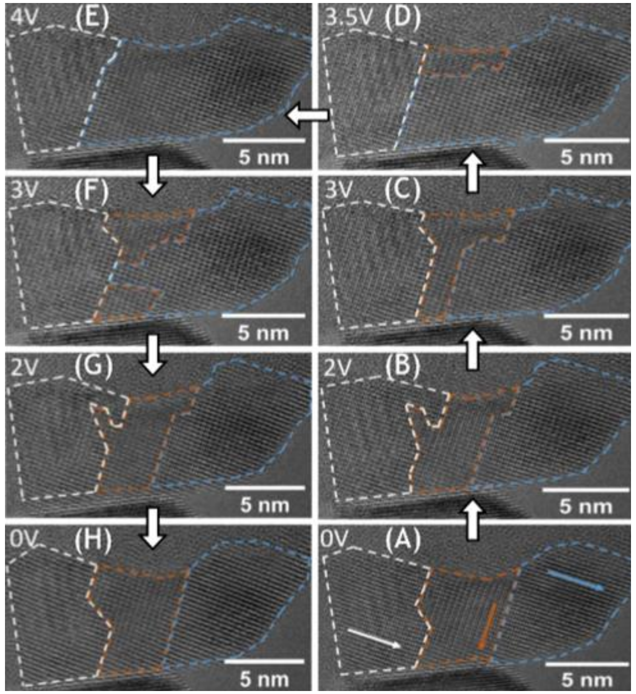
Memorizing synaptic weight

Triase+™ EX-II™ MS: Multi-source Supply for Controllable Film Composition

Under development

Ferroelectric properties

HfO_2 (linear)	HfZrO (ferroelectric)	ZrO_2 (antiferroelectric)
		



In-situ TEM measurement with simultaneous voltage cycling of antiferroelectric ZrO. Crystal grains grow and shrink by field driven domain wall migration as the voltage cycles from 0V→4V→0V.

Demonstrated at TEL Technology Center, America.

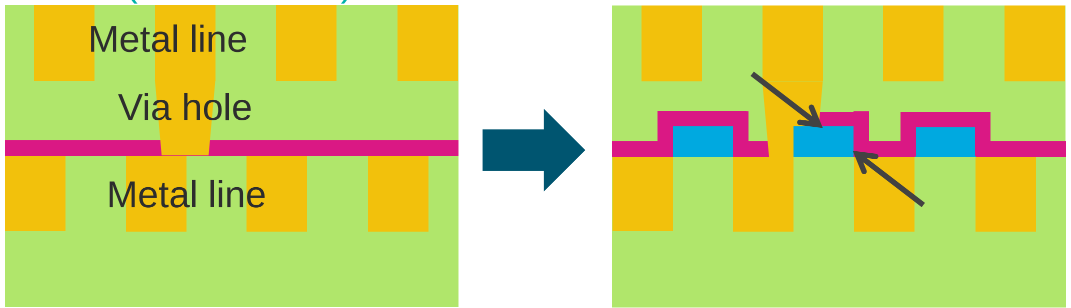
Reference: Lombardo *et al.*, VLSI 2020

Multi-source supply enables controllable film composition, making possible the formation of various functional films

New Opportunity: Area Selective Deposition for Sustainable Scaling

- Features
  - Selective growth of film on metal/dielectric surface
  - Excellent surface pre-treatment technology for high selectivity between growth and non growth surfaces
- Applications
  - Logic BEOL, Fully Self-Aligned Via (FSAV)
  - To every scaled patterning for enhancing lithography misalignment margin

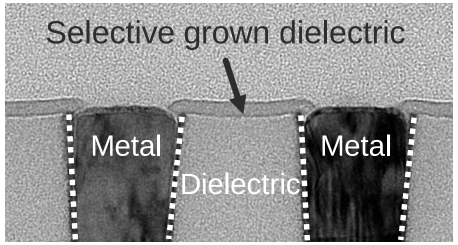
Conventional interconnects (without ASD) | Fully self-aligned via (with ASD)



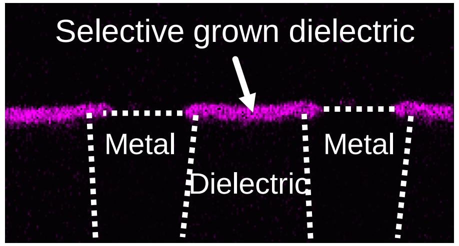
Area selective deposition (ASD)

Selective growth film

Cross-sectional image by TEM



Elemental mapping by EDX



@TEL internal structure

Reference: S. Azumo, 32^{nd} symposium, SCEJ

Summary

- TiN for super high aspect ratio
  - Sustains DRAM capacitor scaling
  - Enhances word line performance in 3D NAND
- High quality high-k dielectric
  - Newly adopted for DRAM peripheral high-k metal gates
  - Enhances control gate performance in 3D NAND
- Multi-source supply
  - Realizes controllability of film composition
- Area selective deposition
  - Enlarges misalignment margins in patterning

Triase+™

TEL's Strategies toward Digital Transformation

January 20, 2021

Noritaka Yokomori
Deputy General Manager, Corporate Innovation Division

TEL's Vision for Digital Transformation

- Industry as a whole is increasingly adopting digital transformation (DX), and the semiconductor industry is no exception. DX occupies an important position as one piece of the solution to demand for further scaling and multi-layering

AI chips

Autonomous

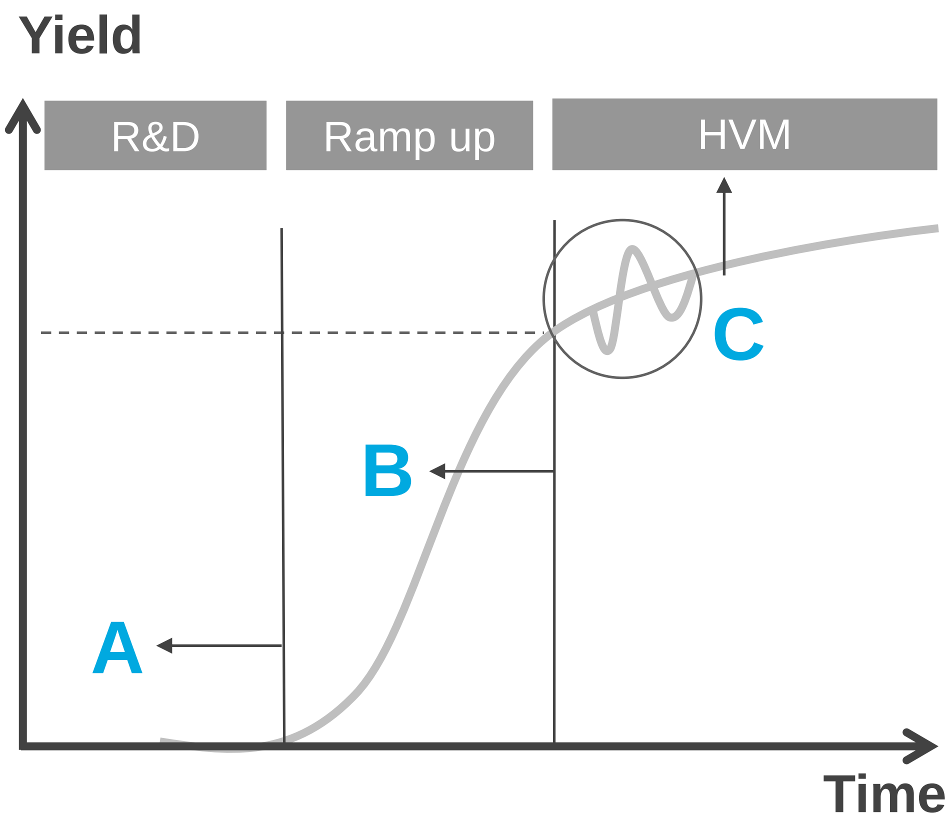
Cloud services

AR/VR

TEL DX Vision

A global company where all employees drive enterprise value creation sustainably through activities such as value addition and efficiency improvements by leveraging digital technology

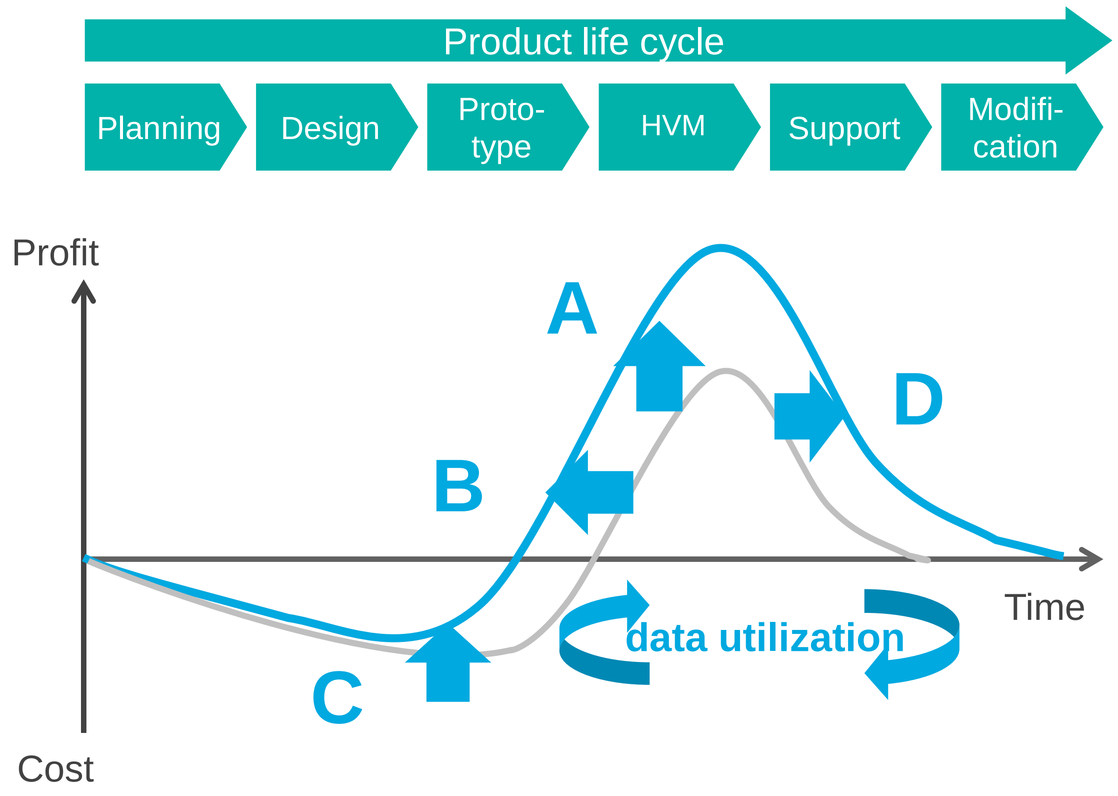
DX in Contributing to Customers' Value Creation



Potential Application		Example
A	**Shorter R&D TAT**	Swift POR proposal via accurate simulation
B	**Shorter ramp up**	Chamber-to-chamber matching, automatic adjustment functions
C	**Improved productivity/yield**	Predictive maintenance, fault detection, process adjustment functions via monitoring and analysis functions

From development to production, contributes to customers' value creation in a range of settings

DX in Raising Capital Efficiency



	Potential Application	Example
A	**Higher profitability**	Provide high value-added products that contribute to customers' value creation
B	**Shorter time to market**	Shorter development period through more efficient development environment
C	**Lower production cost**	Lower number of prototypes by using simulation
D	**Extended lifetime value**	Propose appropriate maintenance/modifications

From product planning to maintenance,
raises capital efficiency in a range of settings

DX Activities

Digital enablers

- High-performance computing
- Cloud infrastructure
- AI technology
- IoT, xR

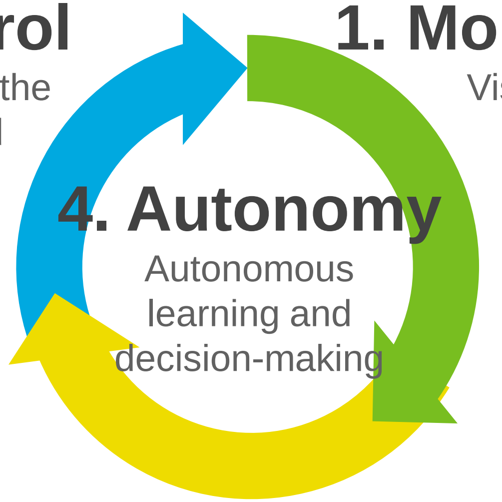
Surrounding environment

- Progress in data sharing and collaboration in supply chains
- High expectations for AI and robot support of humans

Added value creation/improved capital efficiency

3. Control
Feedback to the real world

1. Monitoring
Visualization



2. Analysis and prediction
Analysis and prediction with digitalized data

Achieving goals

- Resolution of high value problems

High value problem

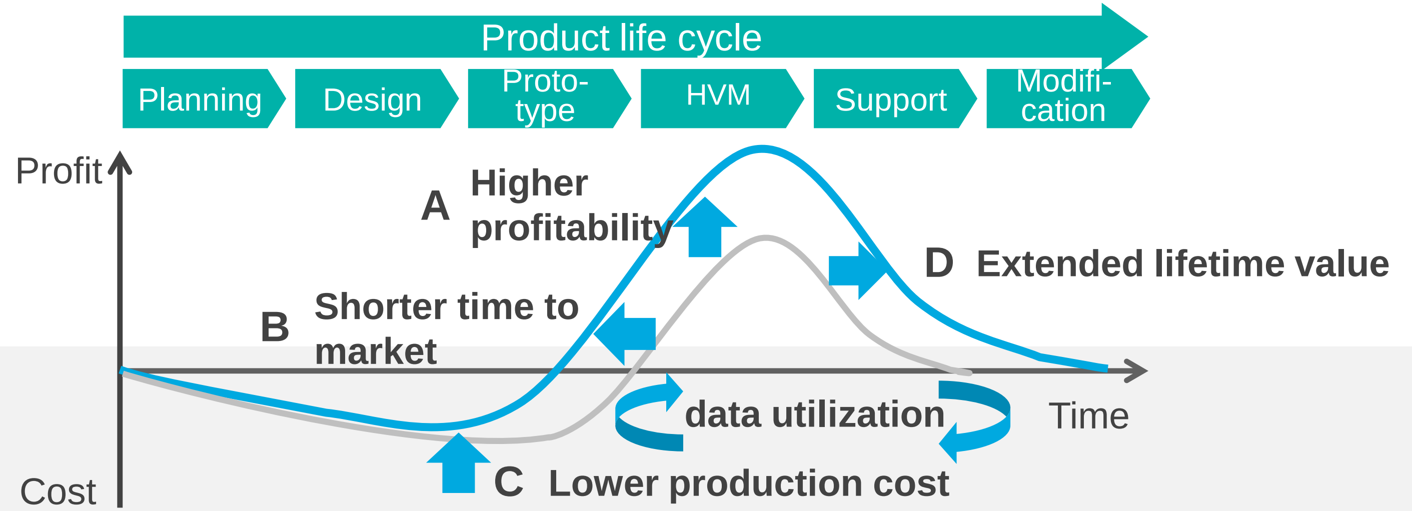
- **Quality**
- **Cost**
- **Speed**
- **Productivity**
- **Energy consumption**

Digital transformation in resolving high value problems

Overall Image of TEL's DX Project

Application

Develop applications that contribute to creation of corporate value via DX infrastructure



DX Infrastructure

Create DX infrastructure for a platform for skills/culture/data application

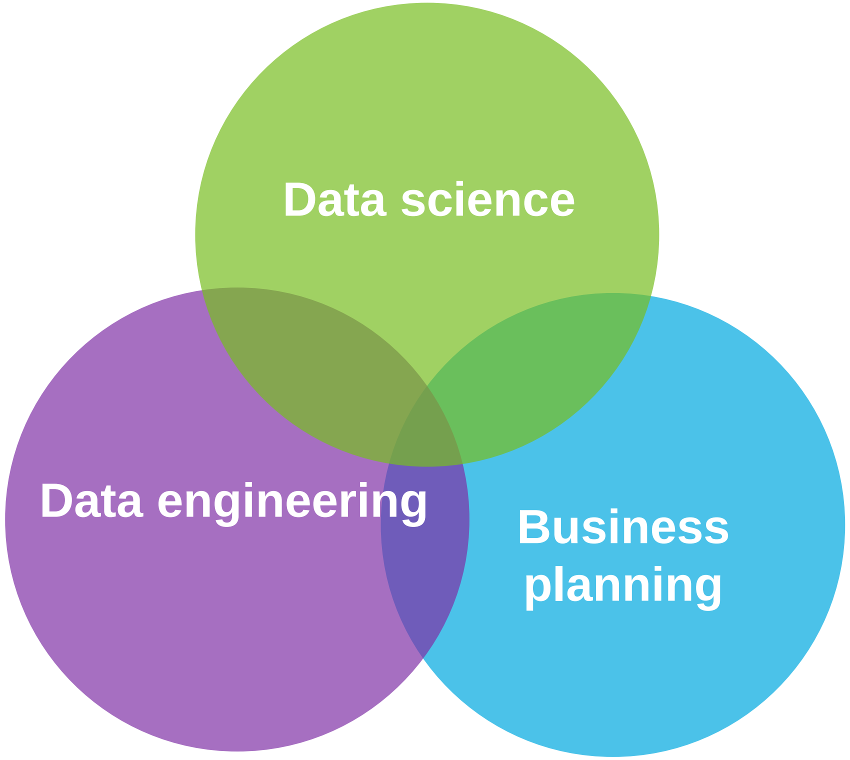
Improving skills

Fostering consciousness/culture

Creating environment
(Governance/data plafform)

Utilize DX infrastructure to develop applications that create corporate value

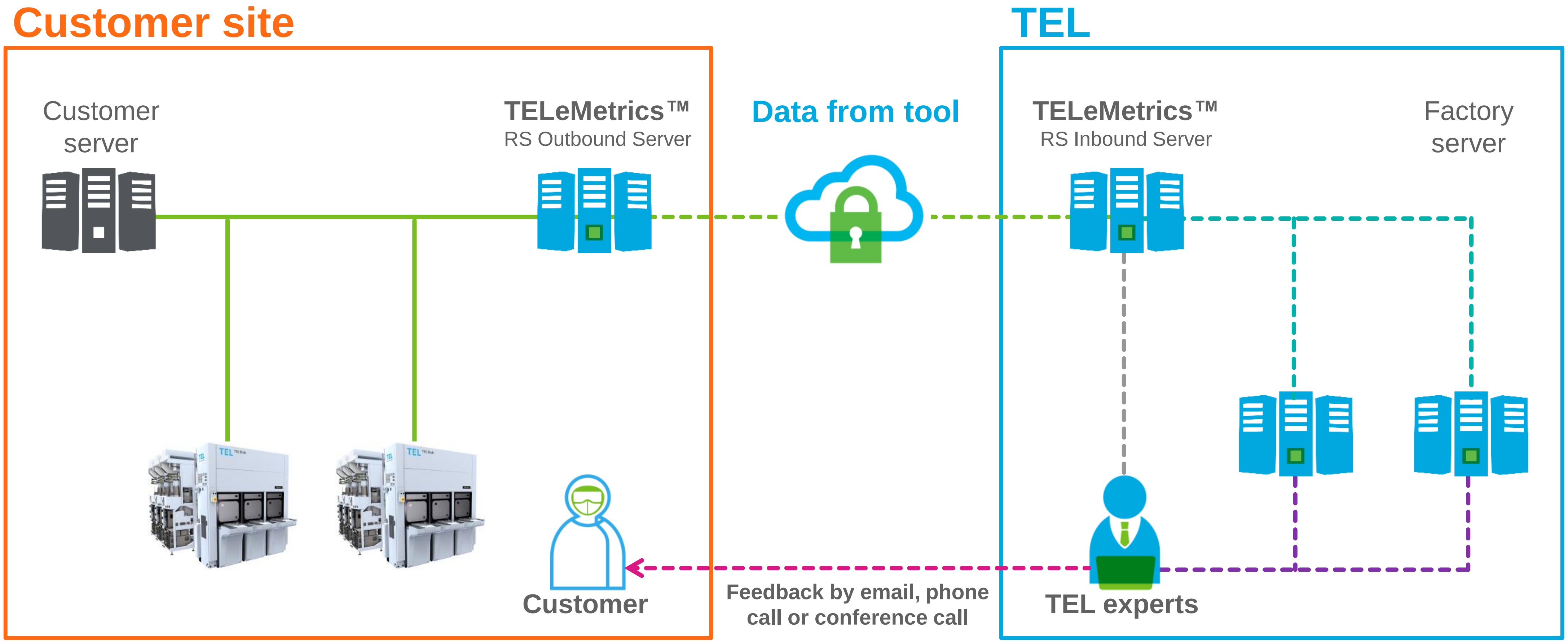
DX Engineer Training Plan



Data science	Ability to understand and utilize data science, such as data processing, AI and statistics
Data engineering	Ability to give meaningful shape to data science for TEL's efforts to create corporate value, and to implement and operate in line with targets
Business planning	Ability to evaluate issues and their context, implement measures to resolve them, and link this to business (earnings ability)

Systematically train human resources to utilize data science in TEL's business

TELeMetrics™: Remote Connection with Customer Fabs



Transformation from selling man-hours to selling value

Remote Support Using AR

Customer's cleanroom

Using smart glasses

TEL support center

AR: "Augmented reality"; technology that can overlay information on a view of the real world via smart glasses

Apply new technology in this era of big data to enhance service efficiency

Exploring Materials Through AI

A way to co-optimize process requirements and materials

Materials informatics

Academic papers

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Materials database

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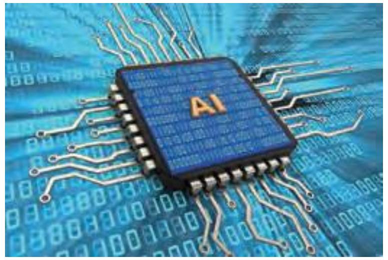
Data science



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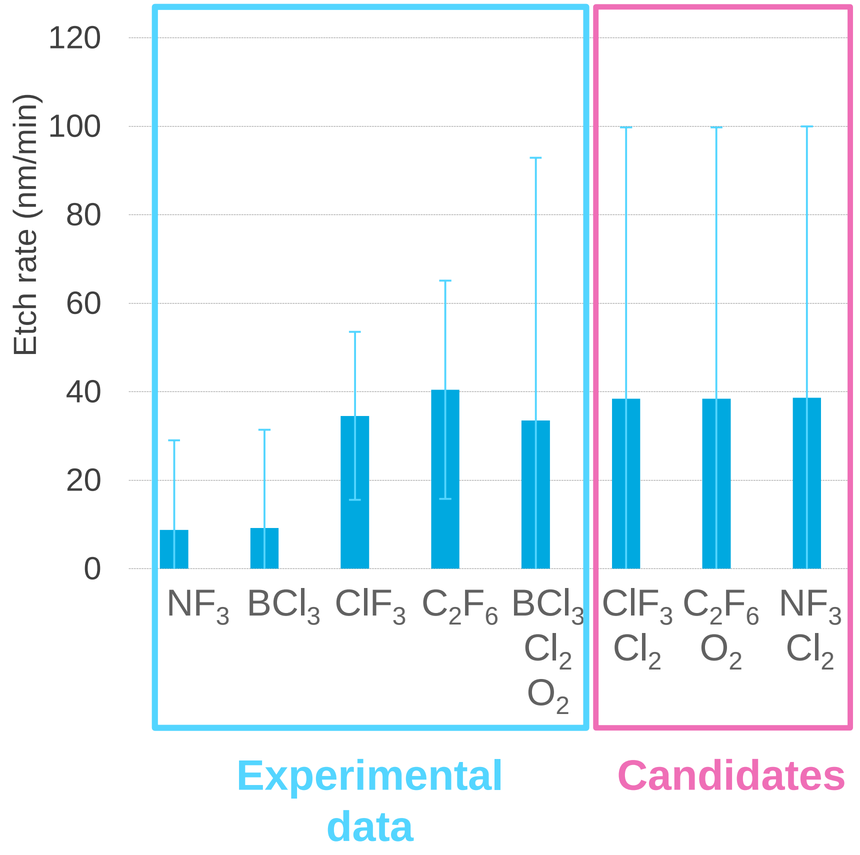
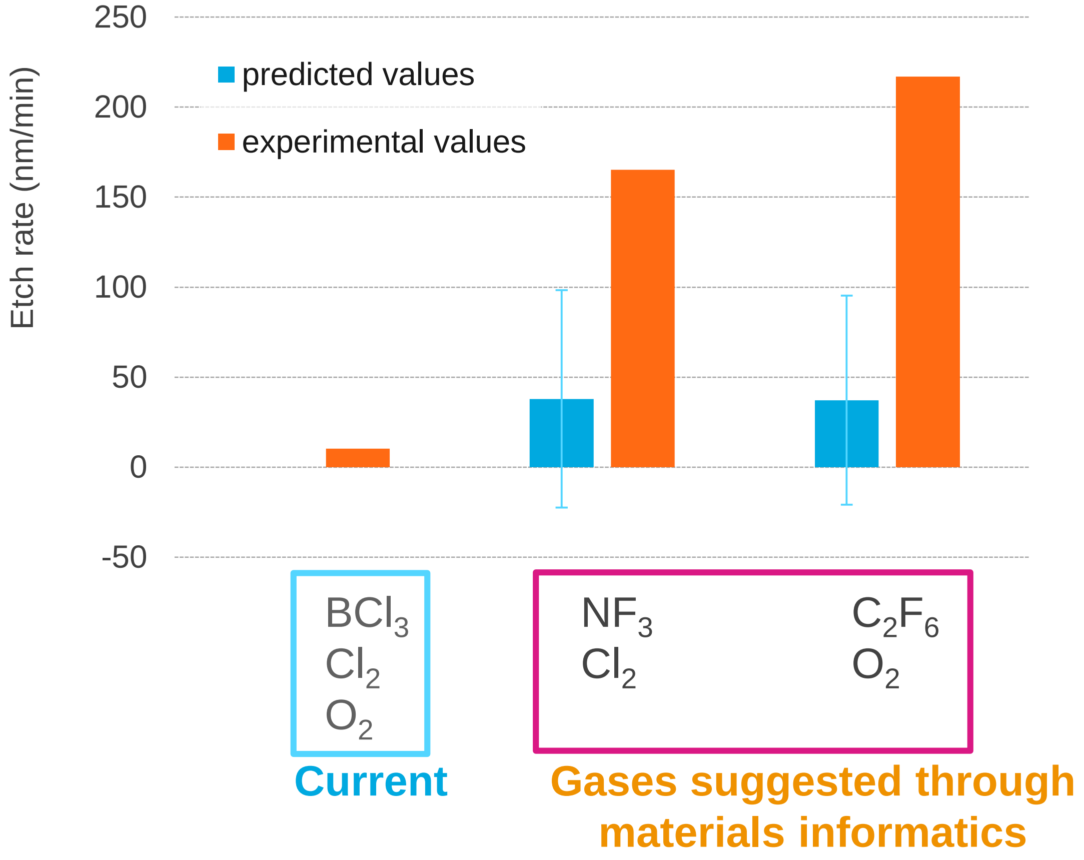
Experiment

Explore materials for use in etching metal oxides

Comparison of Predicted and Experimental Values

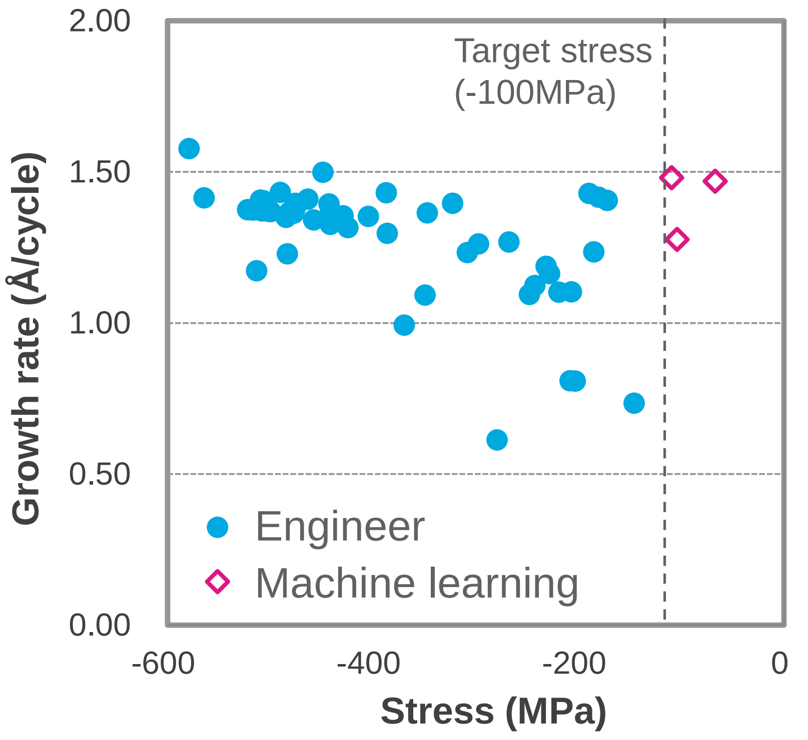




Gases with higher etch rates than before were suggested using machine learning

Process Optimization Through AI

Plasma atomic layer deposition (PE-ALD) film stress adjustment



Process: PE-ALD SiO_2 deposition

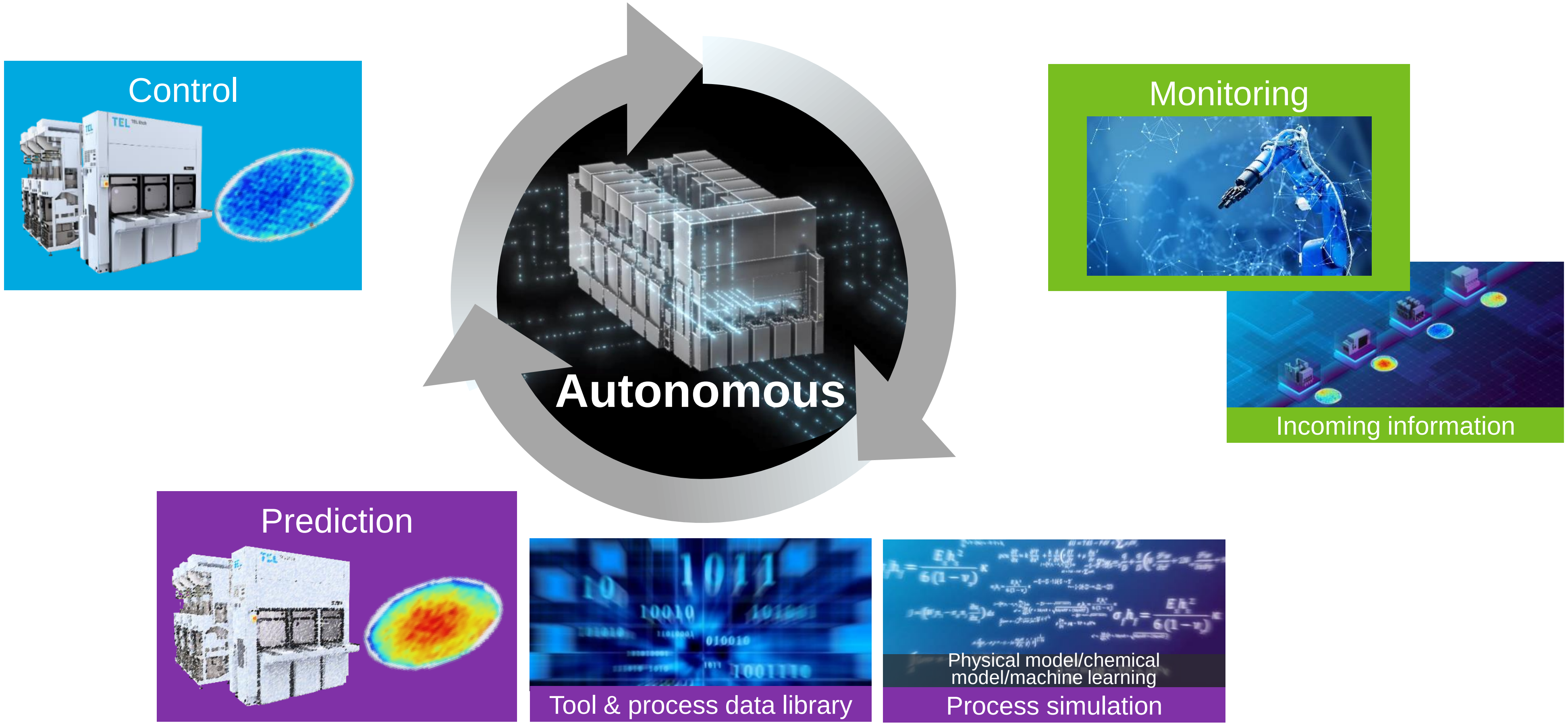
Target: film stress → between -100MPa 0MPa

- Previous method using engineers
  - Unable to achieve target film stress levels
  - Gathered test data, studied with AI

- Optimization through machine learning
  - Achieved target stress levels

Machine learning demonstrated the capability of process optimization

Supporting Customer Value with Autonomous Equipment



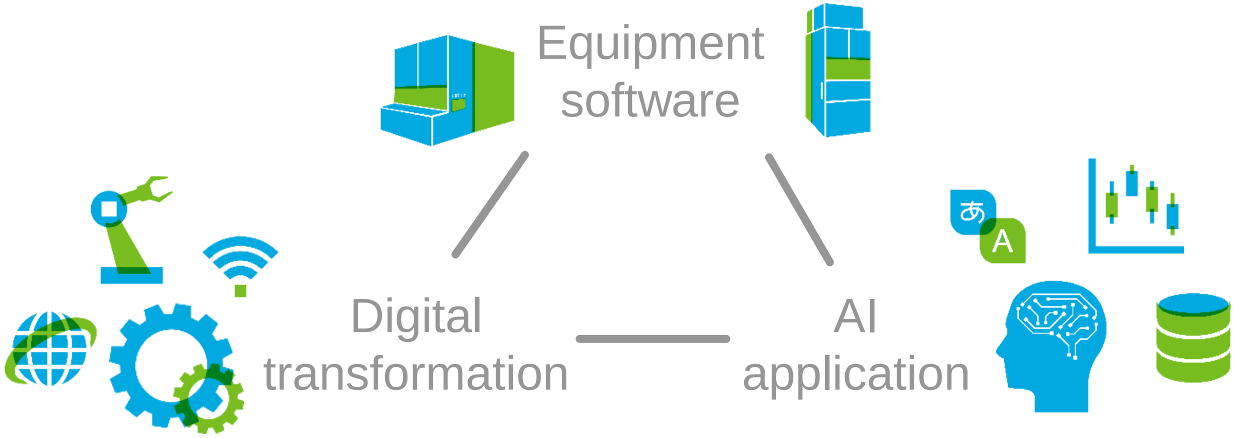
Autonomous learning by gathering necessary information
Equipment senses its environment and state to maintain optimal status

TEL Digital Design Square

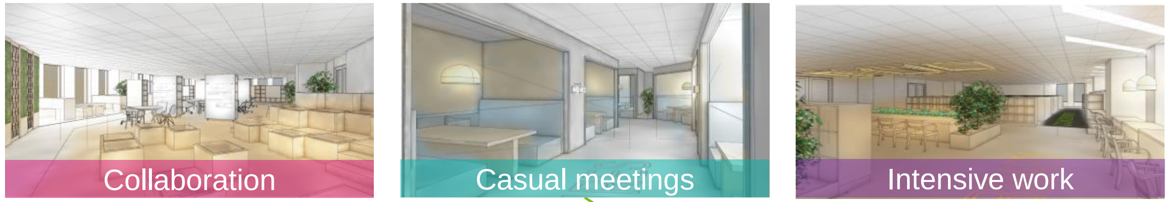
TEL DX Vision

A global company where all employees drive the sustainable creation of enterprise value by leveraging digital technology in activities including adding value and raising efficiency

Development activities



State-of-the-art office



Grand Opening
November 24, 2020
Proudly celebrating 30 years
in Sapporo, Hokkaido, Japan

Opened the TEL Digital Design Square as the home base for DX activities

TEL Digital Design Square Movie

TEL™

TOKYO ELECTRON