TOKYO ELECTRON

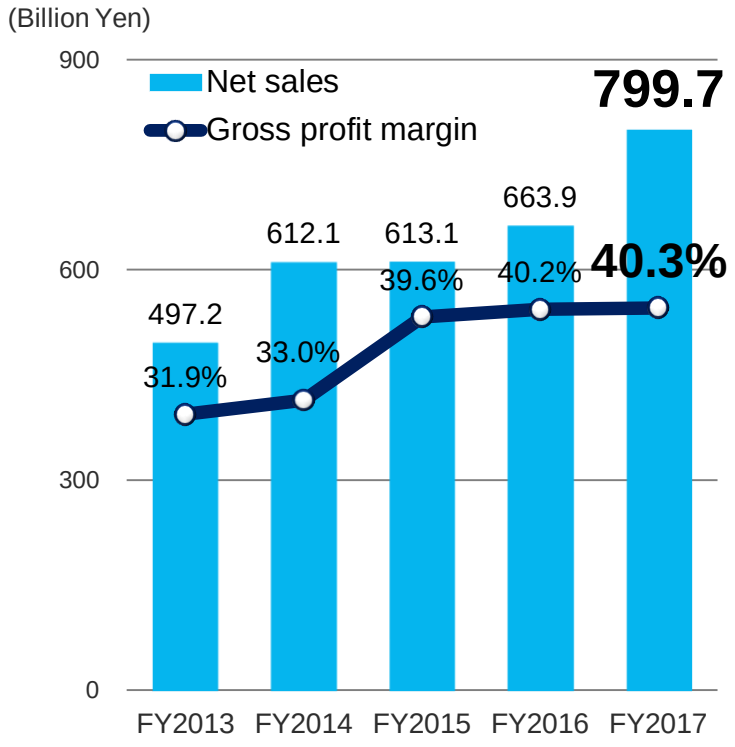
Medium-term Management Plan Progress and TEL Initiatives

May 31, 2017

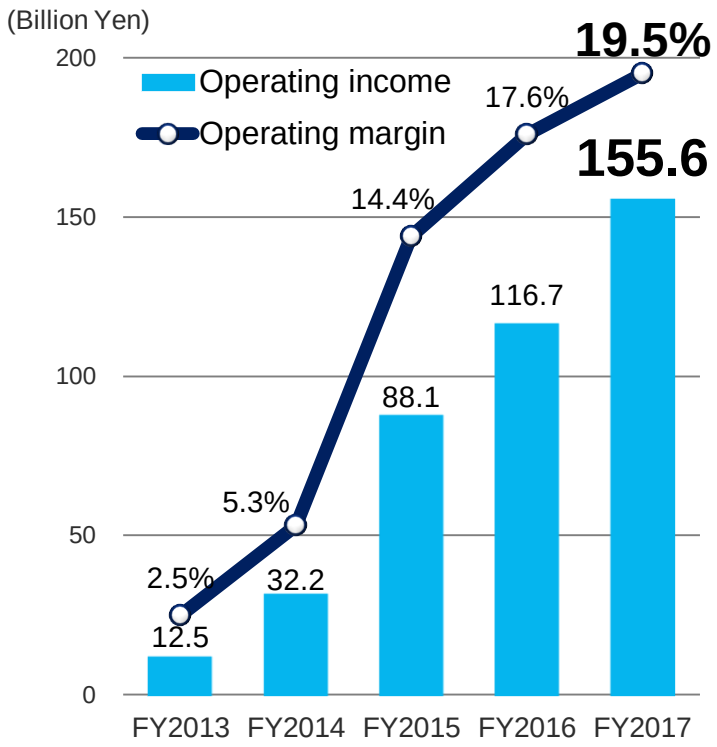
Toshiki Kawai
Representative Director, President & CEO

FY2017 Financial Highlights

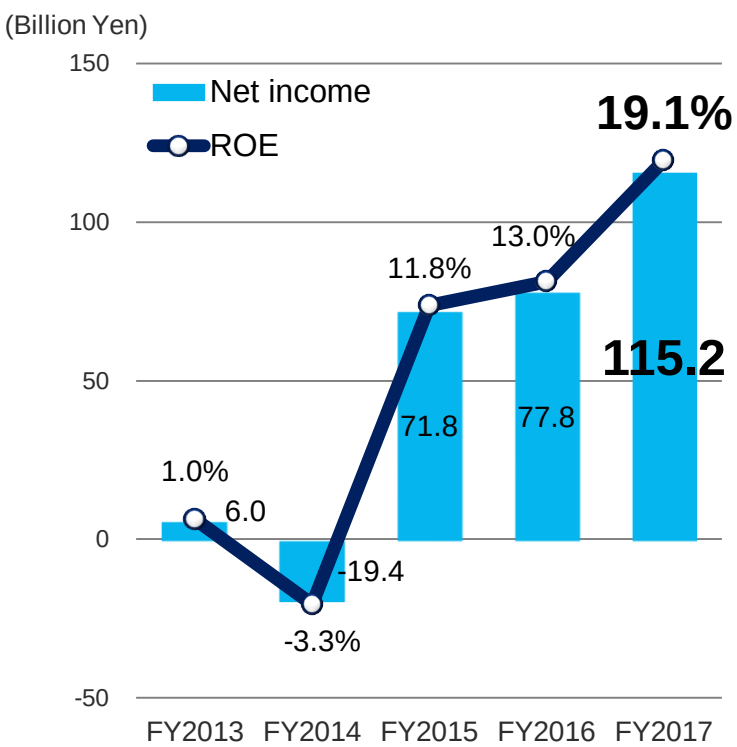
Net Sales and Gross Profit Margin



Operating Income and Operating Margin



Net Income and ROE



- **Net sales increased by 20% YoY, highest ever SPE* sales**
- **Set new record highs for GPM, OPM and net income**
- **ROE of 19.1% (+6.1pts YoY). Further increased capital efficiency**

* SPE: Semiconductor Production Equipment

FY2018 Financial Estimates

(Billion Yen)

	FY2017 (Actual)	FY2018 (Estimates)			
		1st half	2nd half	Full year	Full year YoY change
Net sales	799.7	480.0	500.0	980.0	+22.5%
SPE	749.8	451.0	459.0	910.0	+21.4%
FPD*	49.3	29.0	41.0	70.0	+41.7%
Gross profit	322.2	202.0	210.0	412.0	+89.7
Gross profit margin	40.3%	42.1%	42.0%	42.0%	+1.7pts
Operating income	155.6	104.0	112.0	216.0	+60.3
Operating margin	19.5%	21.7%	22.4%	22.0%	+2.5pts
Net income attributable to owners of parent	115.2	79.0	84.0	163.0	+47.7
Net income per share (Yen)	702.26	481.48	511.96	993.44	+291.18

Expect sales growth to exceed market growth, generating record high profits for second consecutive year

* FPD: Flat Panel Display Production Equipment

Current Progress with Medium-term Financial Targets

WFE*	FY2015 (Actual)	FY2016 (Actual)	FY2017 (Actual)	FY2018 (Estimate)	Medium-term financial targets	
Market size	$31.9B	$31.4B	$35B	$38B	$30B	$37B
Net sales	¥613.1B	¥663.9B	¥799.7B	¥980.0B	¥720.0B	¥900.0B
Operating margin	14.4%	17.6%	19.5%	22.0%	20%	25%
ROE	11.8%	13.0%	19.1%	-	15%	20%

Steady improvement in results.
Continue to focus on improving profit margins

* WFE (Wafer Fab Equipment): The semiconductor production process can be divided into two sequential sub-processes: front-end (wafer fabrication) and back-end (assembly and test) production. WFE is used in the front-end production process. Equipment for wafer-level packaging is not included in the WFE market size here.

Outperform the Market

- **Continue to achieve earnings increases greater than market growth**

  FY2017 results (compared to FY2016)

  ⇒ TEL sales growth **+20.4%** (WFE market growth* +**11.5%**)
  Operating income growth **+33.3%**

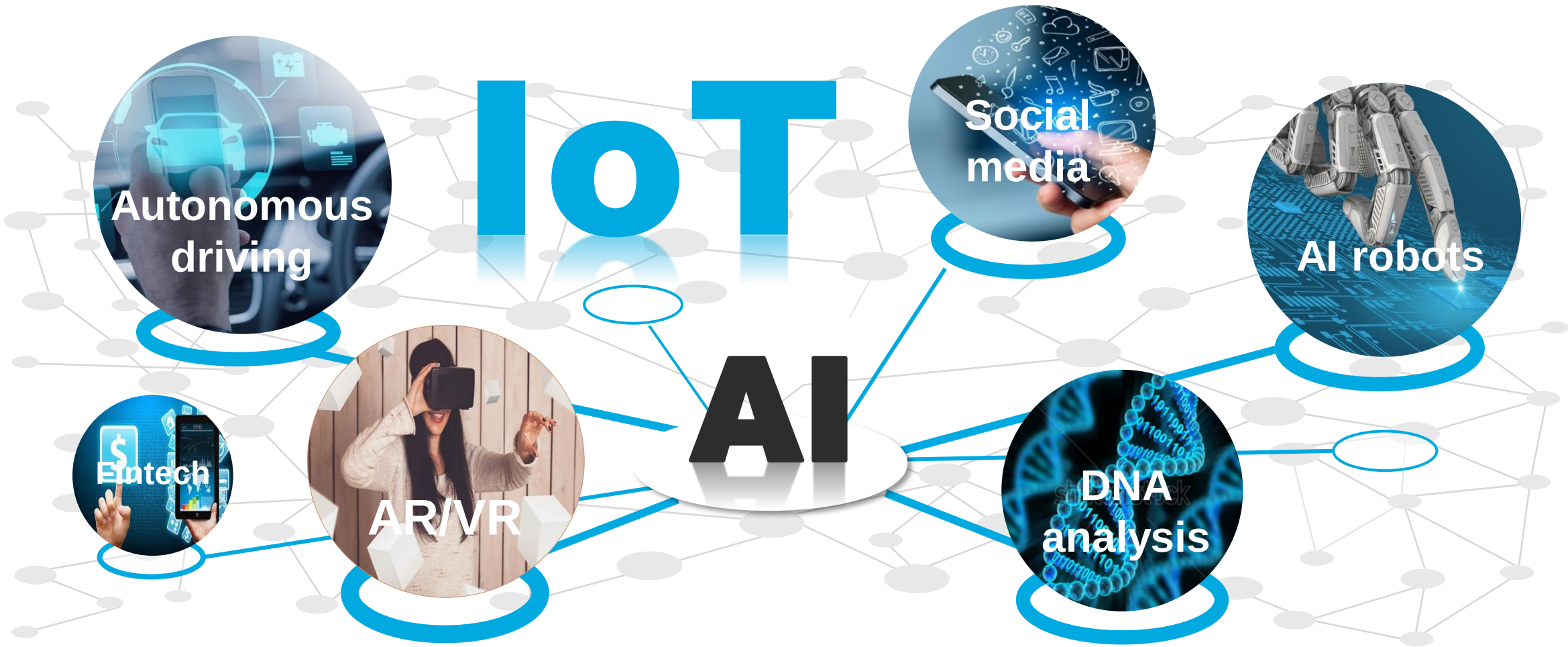
  FY2018 plan (compared to FY2017)

  ⇒ TEL sales growth **+22.5%** (WFE market growth* +**8.6%**)
  Operating income growth **+38.7%**

* WFE market growth rates are for the calendar year

- **Expand market share for etching system, thermal processing system, and cleaning system**

Era of IoT



The amount of data is dramatically increasing with the growing number of connected devices

Infrastructure Evolution Supporting the IoT Era

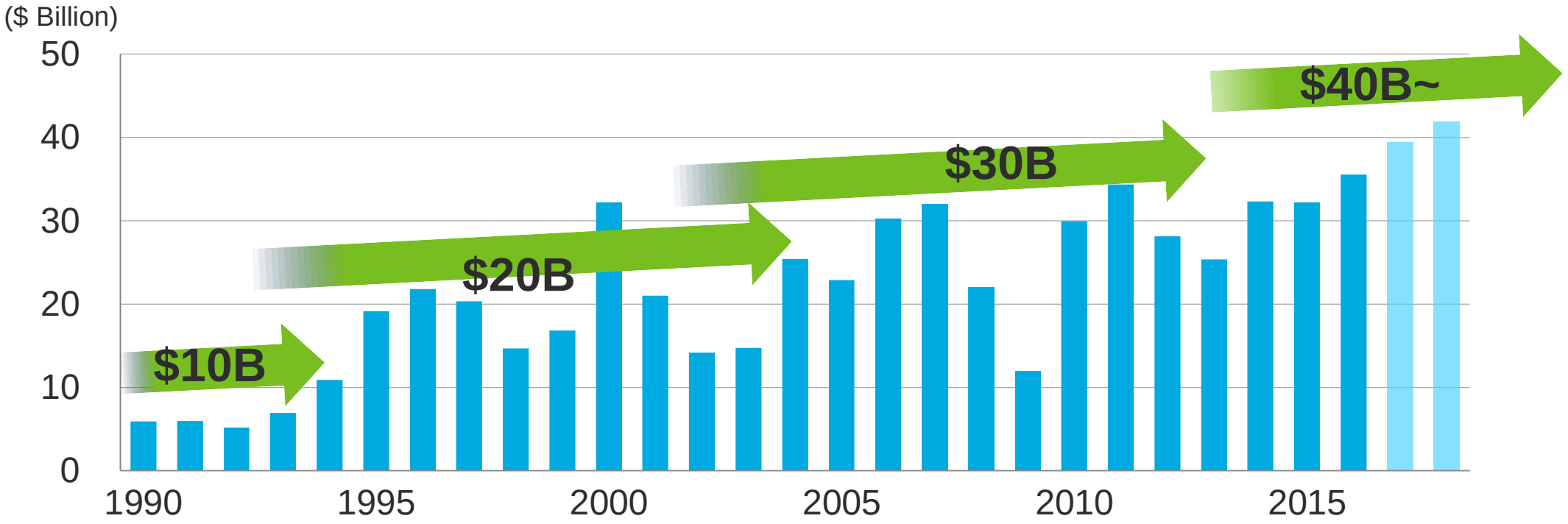
5G, the next generation communications standard, will establish the infrastructure for an IoT society

The Evolution of Society

Semiconductors will be increasingly integrated throughout society

Expansion of WFE Market

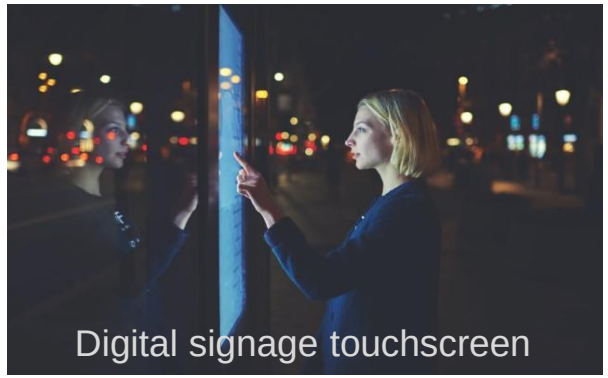
Equipment for wafer-level packaging is not included in the WFE market size here



Source: 2001-2013 SEMI
2014-2018 VLSI "Chip Market Research Services Equipment Database, 1Q17 Update" Apr. 2017. Graph created by TEL using above data

Semiconductor industry is heading for its next growth phase

Growing Use of Displays as Interface Devices



Functionalities sought in displays:

ultra-high resolution・large scaled・
low power consumption・flexibility

Further growth expected in the display market

New Medium-term Financial Targets (toward FY2020)

Equipment for wafer-level packaging is included in the WFE market size here

WFE Market size	$42B	$45B
Net sales	¥1,050B	¥1,200B
Operating margin	24%	26%
ROE (Return on Equity)	20-25%	

Targets adjusted due to changes in market conditions

New Organization: Development & Production Group

As of June 1, 2017

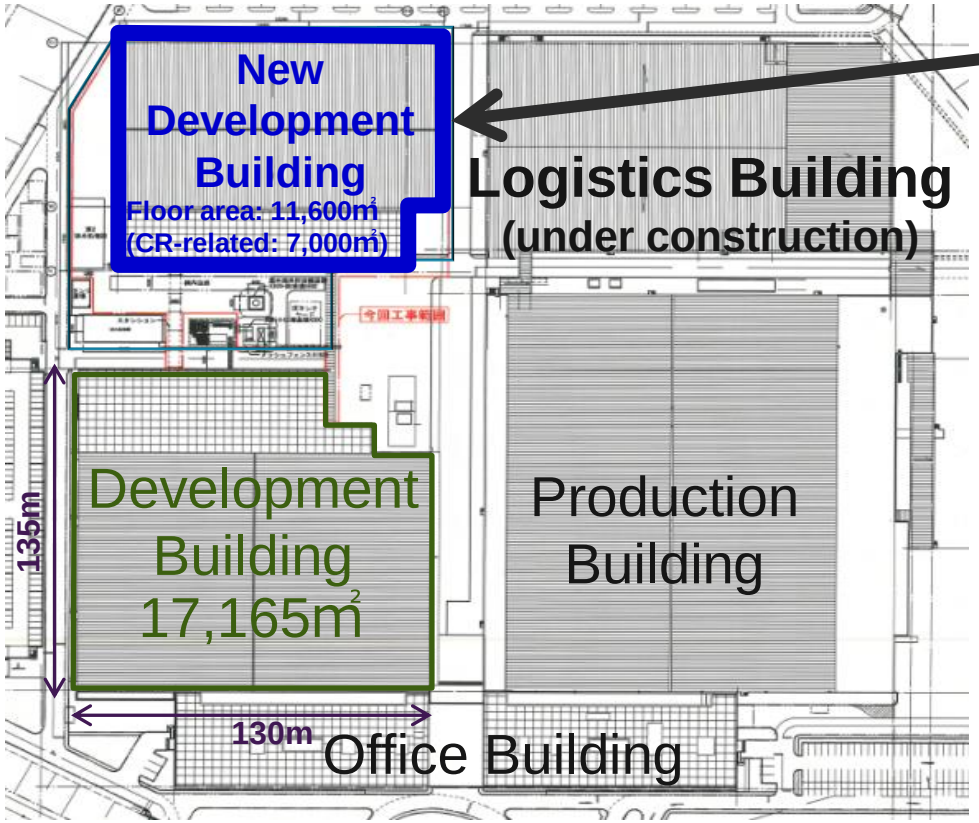
- **Improve development flexibility as we enter new growth phase**
- **Merge Yamanashi and Tohoku plants, establish TTS***
  - Combine technology and increase efficiency
  - Move process integration functions to plants, accelerate commercialization
- **Technology Strategy Division to advance future technologies/technological integration focused on the IoT era**

President & CEO
Toshiki Kawai

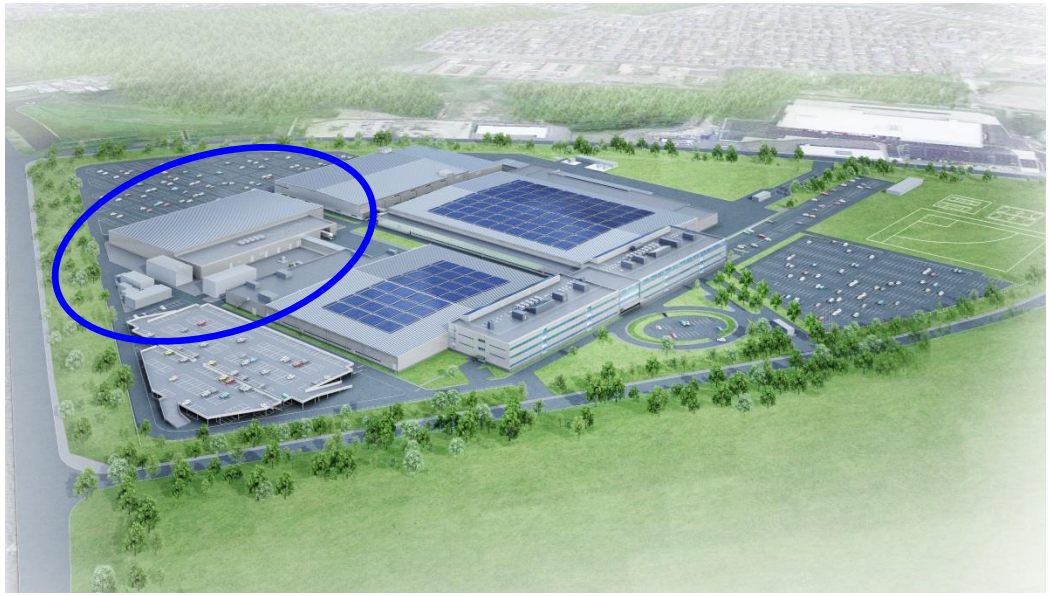
Development & Production group	Main products
Dev. & Production 1st Division	Deposition systems
Dev. & Production 2nd Division	Etching systems, Dry cleaning systems
Dev. & Production 3rd Division	Coater/developers, Wet cleaning systems
Dev. & Production 4th Division	Test systems, FPD dry systems
Technology Strategy Division	

* TTS: Tokyo Electron Technology Solutions Ltd.

Miyagi Plant: New Development/Logistics Buildings



New development building: construction scheduled for completion by the end of August, 2018



Tokyo Electron Miyagi Ltd.
New development building and logistics building

Create and optimize customer value through joint R&D with customers, R&D integration, and continued improvement

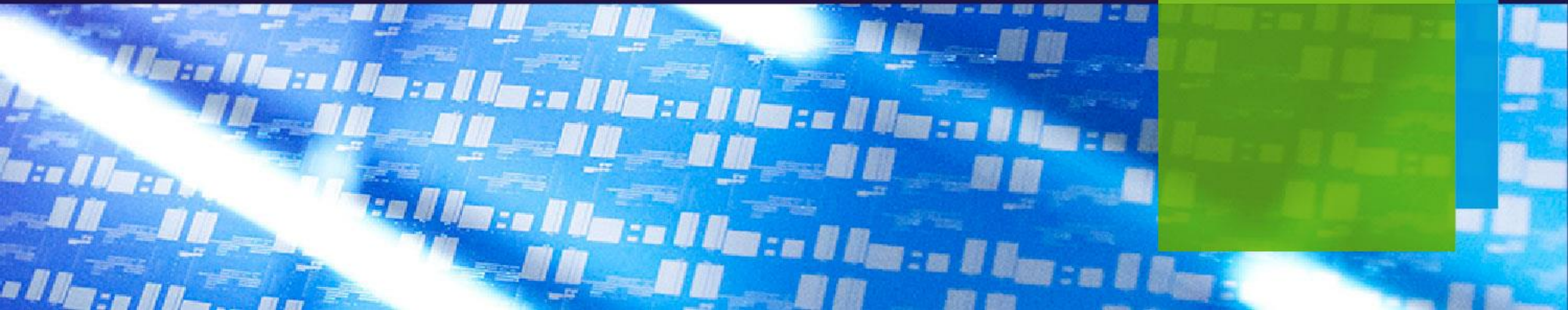
Summary

- **Semiconductors and FPDs entering a new growth phase**
  - Revised WFE market outlook and financial targets (market outlook of $42B-$45B)
- **Optimize R&D structure to adapt to future business environment**
  - Establish five development divisions, ensure a flexible development structure
  - Establish TTS to strengthen deposition business (technology integration/efficiency)
  - Move Process Integration Center to TTS, accelerate product development
- **Expand etching business to respond to further growth**
  - Increase production, improve efficiency by constructing logistics building
  - Accelerate development of added-value products by constructing new development building

TOKYO ELECTRON

SPE R&D Strategy

Sadao Sasaki
Representative Director, Executive Vice President & General Manager,
Development & Production Division



Contents

- Growing demand for leading-edge technology: Opportunities for TEL
  - TEL Technology Vision 2030
- R&D strategy progress
  - Demand for leading-edge technology and TEL R&D strategy
  - Unifying development to integrate TEL proprietary technologies
- Medium-term plan: Progress on business focus areas (Etching, Deposition, Cleaning Systems)

Growing Demand for Leading-edge Technology: Opportunities for TEL

TEL Technology Vision 2030

TEL Technology Vision 2030

Semiconductors
for all industries

Energize discussion of future technologies achievable by 2030 and TEL's contribution to these

Building the World of 2030

AI/Deep Learning

Advanced Architecture

Advanced CMOS Technology

Integrated Analog Device

Communication Technology

Image Processing

Edge/Cloud Computing

Storage Class Memory

Charge/Create Energy

Advanced Lithography

Emerging Memory

Critical FEOL/BEOL Solution

Lower Energy Consumption

Material Challenges

Advanced Packaging

Ubiquitous Flexible Display

3D Printing Manufacturing

Intelligent Fab System

Biotechnology

Core Technology

Leading-edge Technology

Customer Satisfaction

Industry Collaboration/Co-Creation

Automatic Operation

Smart Society

CPS/IoT

Personal Medical Robot

Neuromorphic Computing

Environment

Virtual Reality

Rapid growth in semiconductor applications in a range of areas, more sophisticated technology requirements

TEL Growth Strategy

Solution provider for all industries

Solution provider for the semiconductor industry

Current

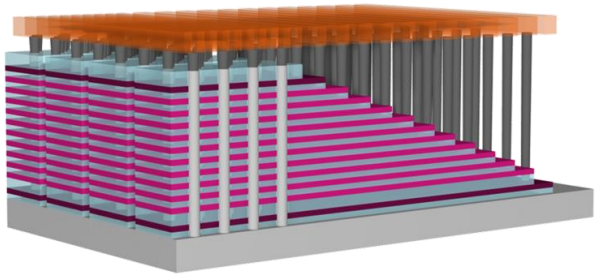
2030

TEL technology contributes to the evolution of semiconductors, the importance of which is growing in all industries

R&D Strategy Progress

Demand for Leading-edge Technology and TEL Strategy

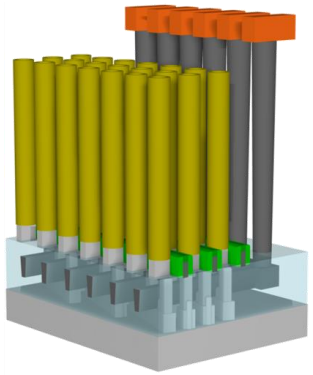
3D NAND



Enhance multi-layering & production capacity

- High selectivity process
- Pursue further process accuracy and improve productivity

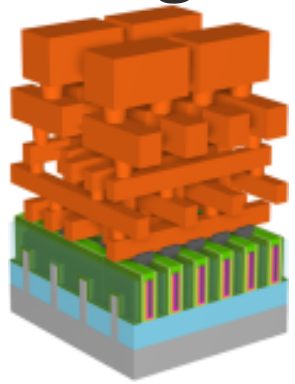
DRAM



Deliver 1X miniaturization

- Improve capacitor performance to further increase storage
- Apply high aspect ratio etching and new materials

Logic

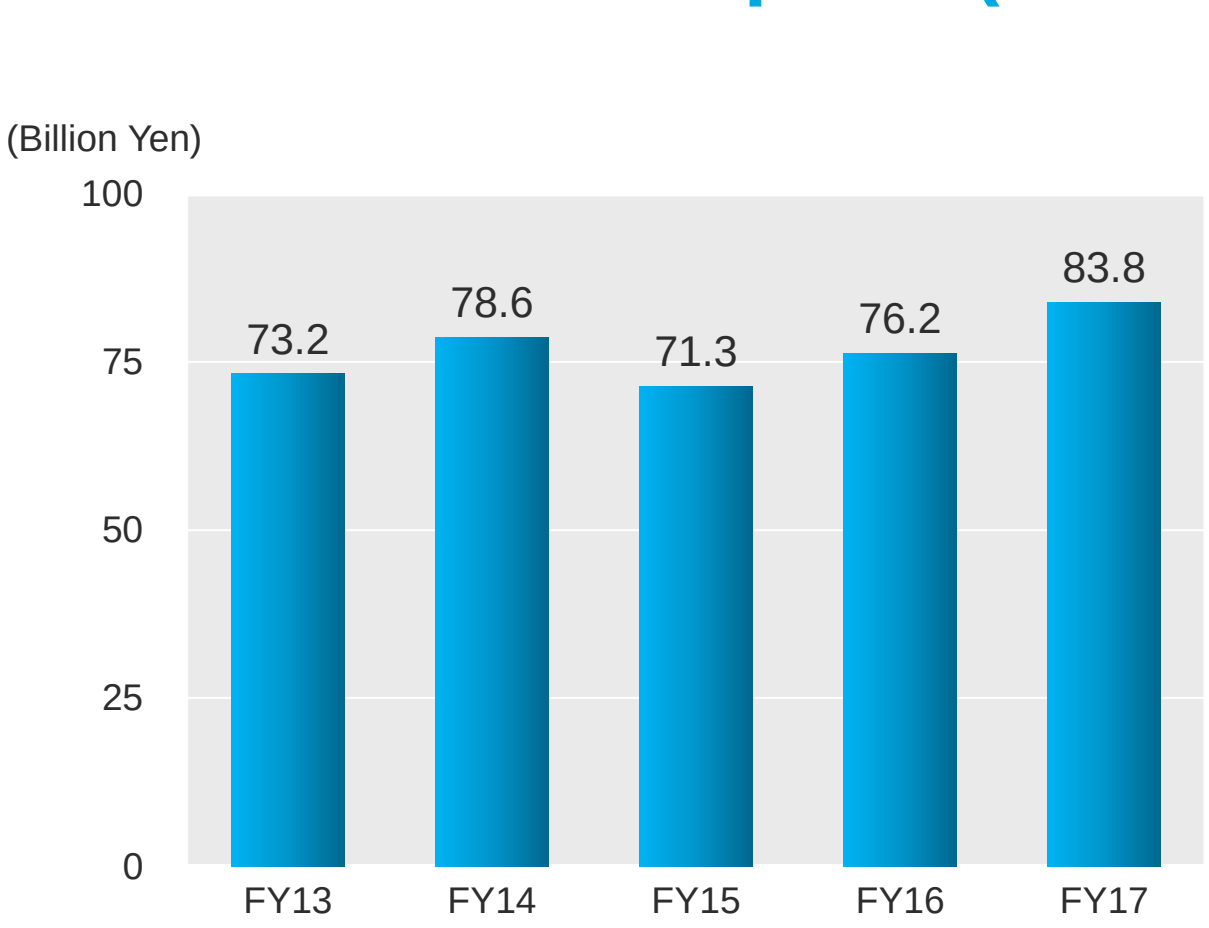


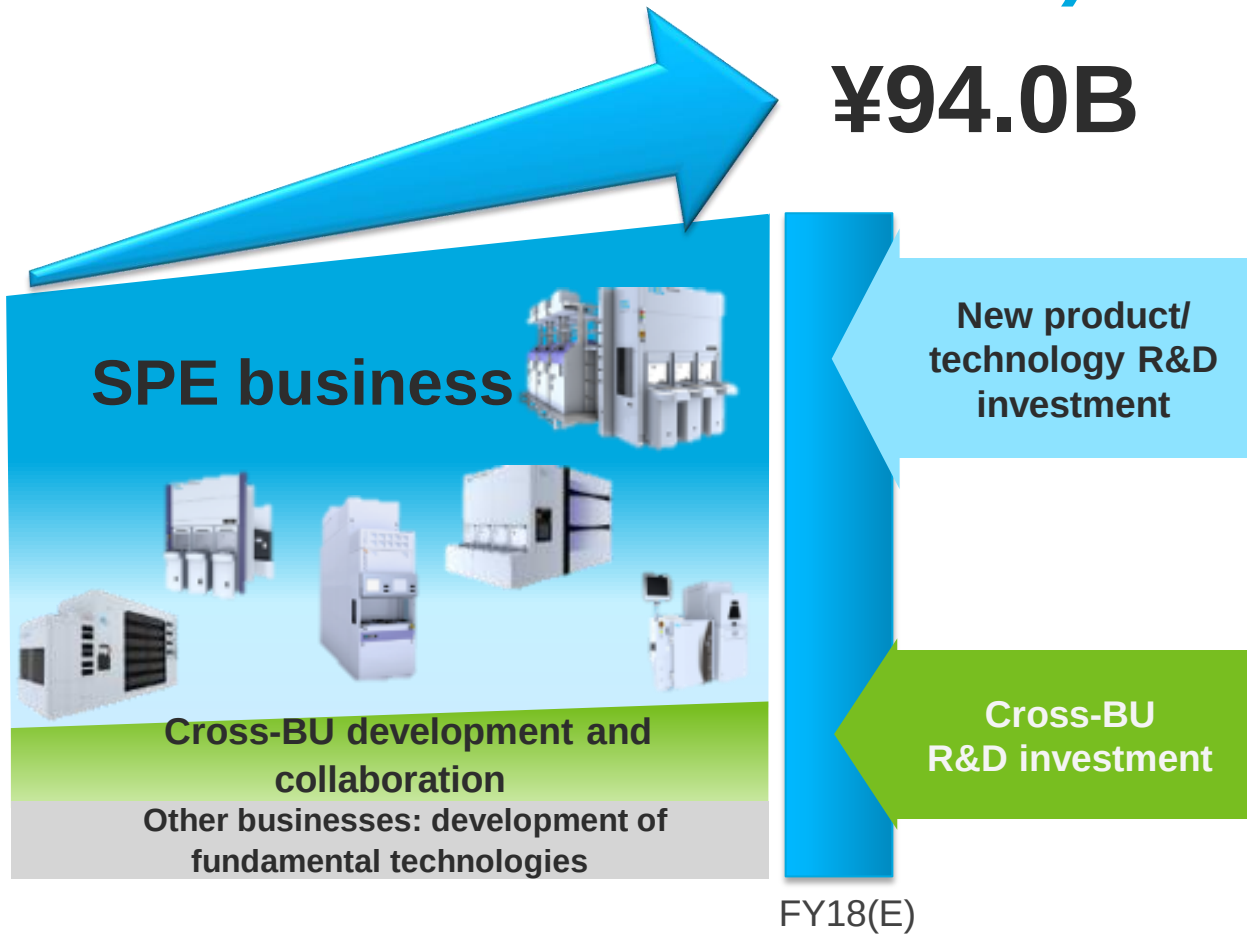
Develop leading-edge 5 & 3nm

- Develop patterning technology for scaling
- Develop new materials, selective deposition

Pursue internal and external collaboration to accelerate development of innovative integrated technologies (process solution development, next-generation platform development)

Increase R&D Spend (R&D Investment in Focus Areas)

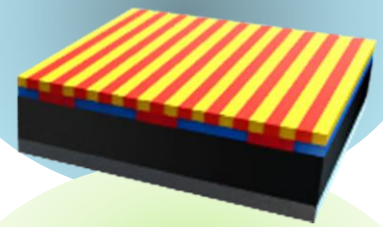




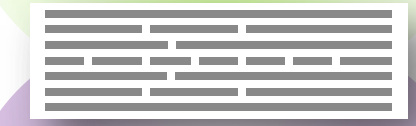
Actively invest in creating further integrated technologies and growth areas

Patterning Strategy

EPE*/CDUchallenges**



Full commercialization of EUV



Limitations of measuring instruments

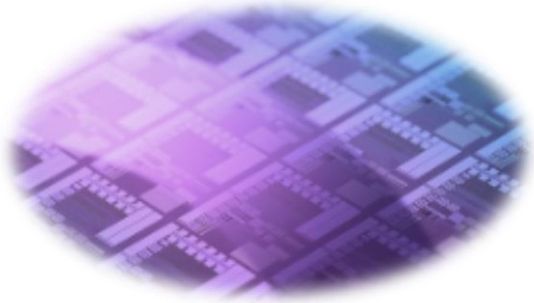
Establish self-aligned patterning technologies with multiple major customers

Advance R&D in close communication with customers
Expand on-site evaluation

Collaborate with leading-edge consortia and equipment/materials manufacturers

imec, SRC, AIST, simulation tool vendors, etc.

Enhance internal evaluation/R&D facilities



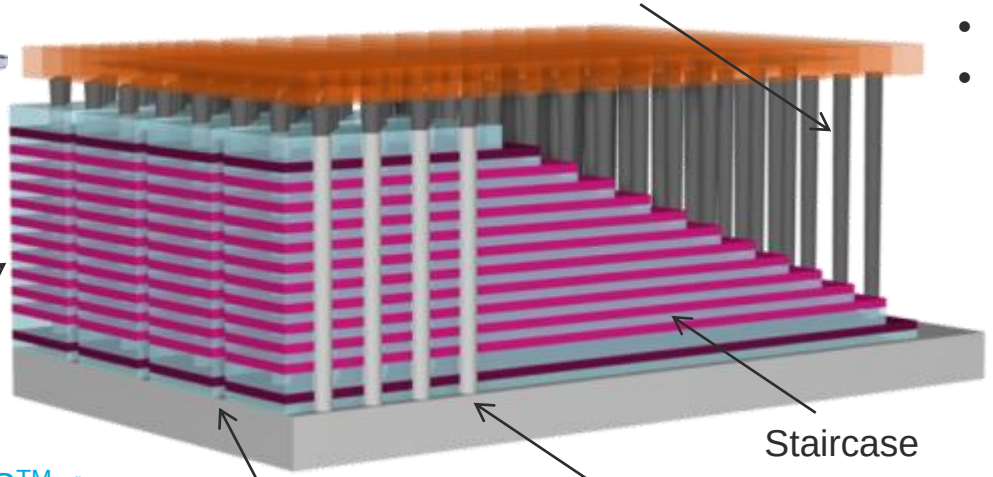
Established Process Integration Center
R&D by function at three facilities (TTCA*, Koshi, Hosaka)**

* EPE: Edge placement error
** CDU: Critical dimension uniformity
*** TTCA: TEL Technology Center, America

3D NAND Key Process Technologies and TEL's Solutions

Plasma dry etch
- Word line isolation
- Channel hole
- Multi-level contact

Tactras™



Lithography
- Word line isolation
- Channel hole
- Multi-level contact
- Staircase

CLEAN TRACK™ LITHIUS Pro™ Z

Chemical dry etch
- Source line pre-clean

Certas™

Thermal process (batch deposition)
- Block oxide (high-k)
- Charge trap (ALD SiN)
- Channel Si
- Cap Si

TELINDY PLUS™

Wet etch
- Replacement word line

EXPEDIUS™-*i*

Atomic layer deposition
- Core oxide

CELLESTA™-*i*

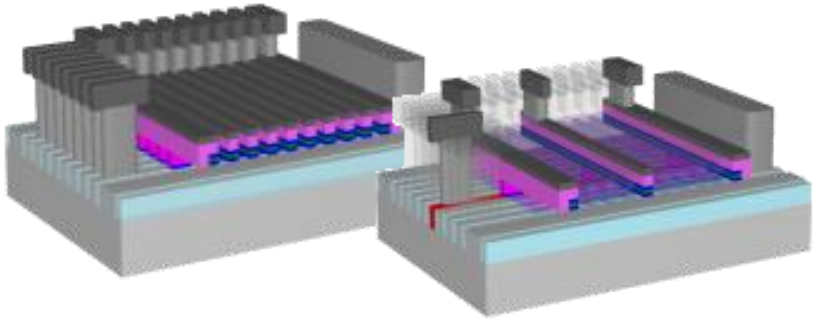
NT333™

Single wafer deposition
- Word line barrier
- Multi-level contact barrier
- Source line barrier

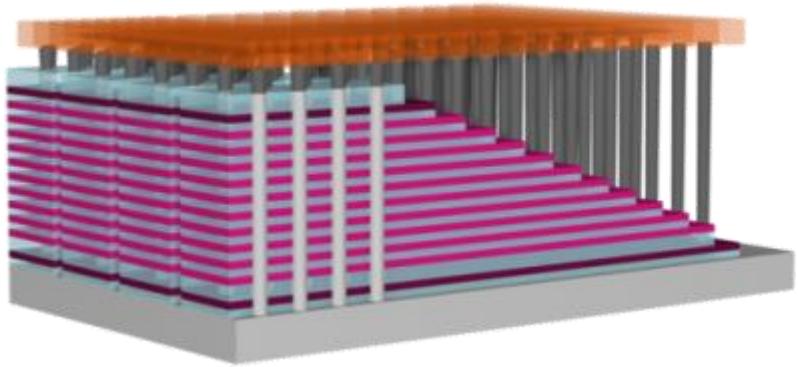
Triase+™

Wet clean
- Bevel clean

Expanding Business Opportunities in the 3D NAND Market

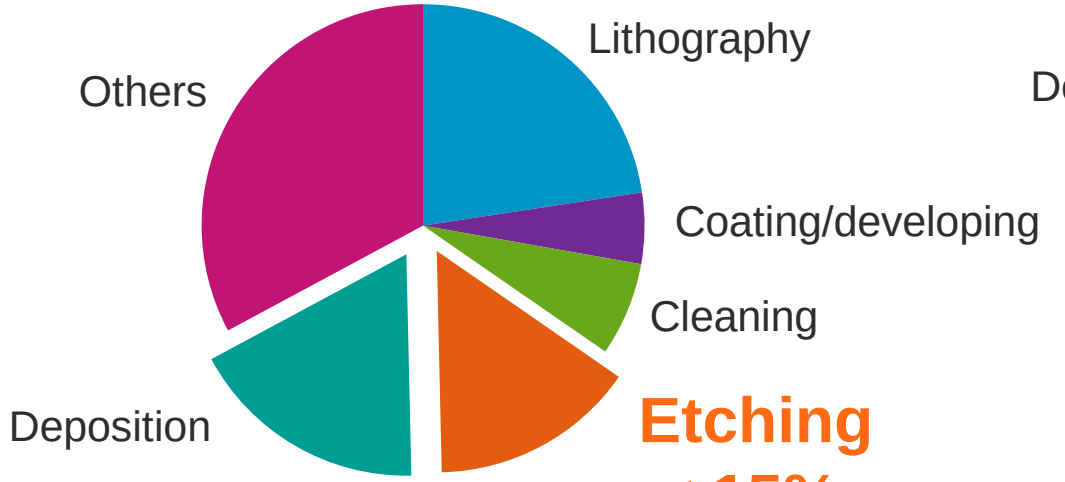


2D
miniaturization

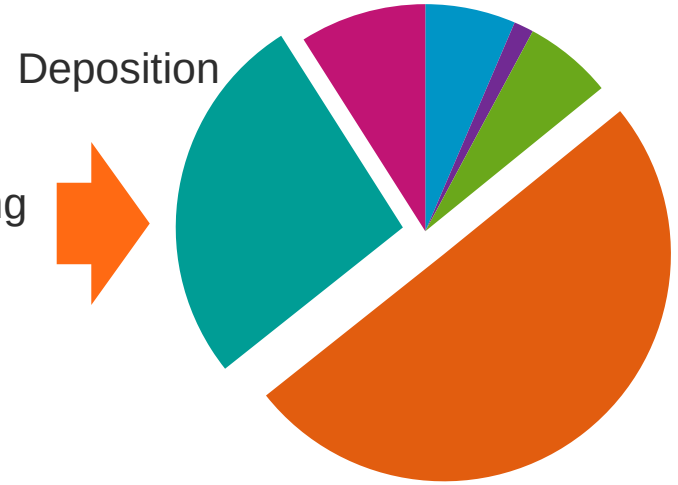


3D NAND
stacking

Equipment ratio for previous NAND capex*



Equipment ratio for 3D NAND*



Multi-layering, high A/R:

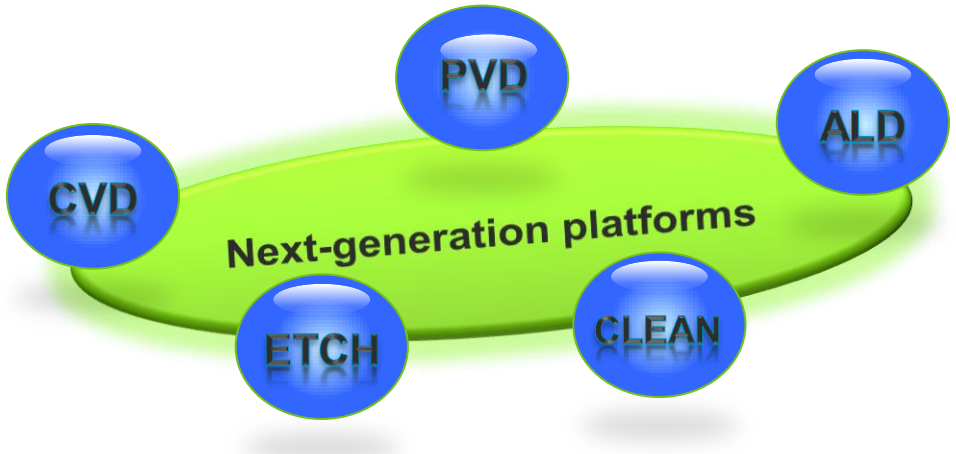
- Increase in number of layers etched
- Pursuit of high process accuracy decreases productivity

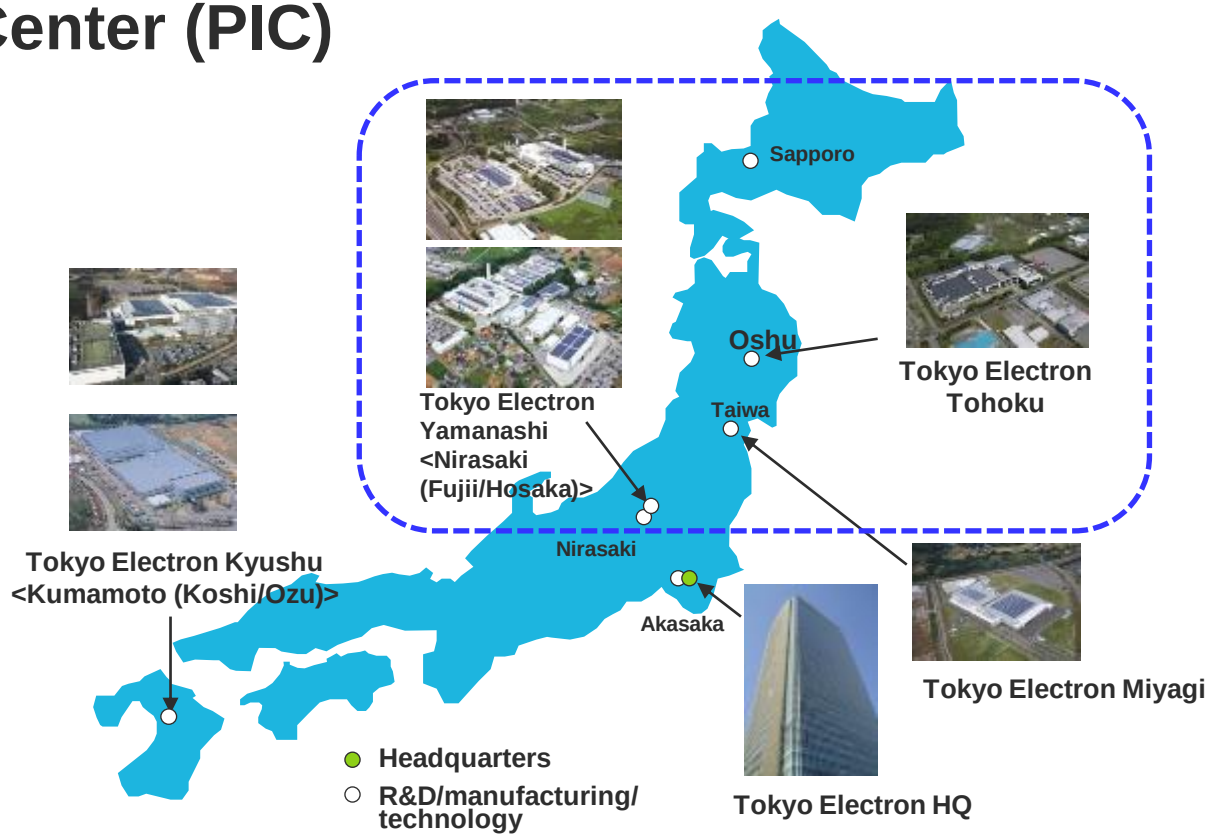
⇒ More equipment units needed

* TEL estimate

SPE Business Strategy: Strengthen Deposition Technology R&D

- **Establish Tokyo Electron Technology Solutions**
  - Unify development resources by merging Tokyo Electron Yamanashi and Tokyo Electron Tohoku
- **Established Process Integration Center (PIC)**
  - Cross-BU process module development
- **Develop next-generation platform**
  - Incorporate new controllers (AI software)





SPE Business Strategy: Deposition Systems

ALD system
NT333™

ALD

Thermal processing system
TELINDY PLUS™

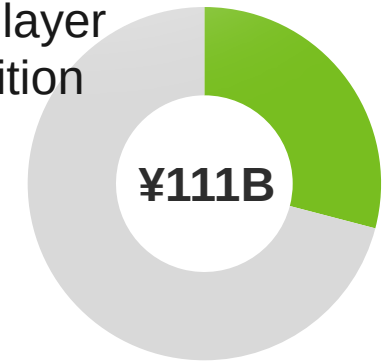
CVD

Single wafer deposition system
Trias*e*⁺™

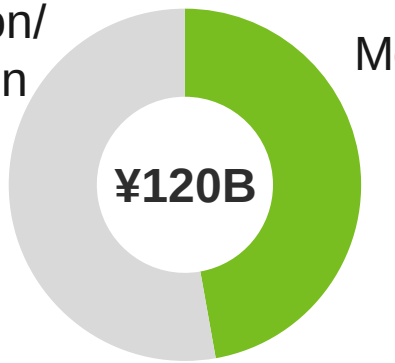
PVD

Sputtering system for next-generation devices
EXIM™

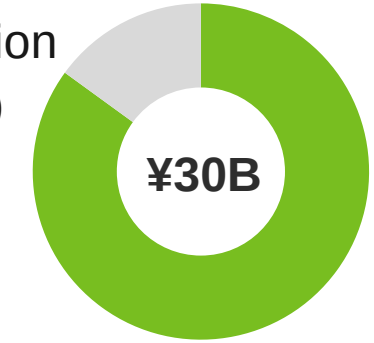
Atomic layer deposition



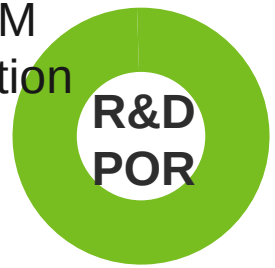
Oxidation/ diffusion CVD (batch)



Metallization (Ti/TiN)



MRAM deposition



Bring together the results of CY2014-16 R&D activities and move to the production preparation stage

Aim to expand earnings based on new technologies for further miniaturization, new structures, and next-generation semiconductors

* Figures reflect TAM estimated by TEL

SPE Business Strategy: Cleaning Systems

- Expand sales of CELLESTA™ single wafer cleaning system
  - Expand applications based on backside and bevel cleaning* and drying technology that prevents pattern collapse during the post-etch cleaning processes
- Secure key 3D NAND processes through batch cleaning
  - Provide high quality and productivity in the metal etching, polysilicon etching, and nitride film removal processes required for precise controllability
- Apply best known coater/developers methods to cleaning system business
  - Share leading-edge technology and expertise by unifying R&D

Single wafer cleaning system
CELLESTA™

Batch cleaning system
EXPEDIUS™

Market share	CY14 (Actual)	CY15 (Actual)	CY16 (Actual)	・・・	CY19 (Target)
Cleaning system	19%	18%	20%		>24%

* Bevel cleaning: process for removing film from the outer part of the wafer

Summary

- Formulated TEL Technology Vision 2030 to facilitate further business growth
  - Capture growth from diversifying semiconductor demand
- Aim for growth through strategic advancement of collaborations with customers and consortia, further strengthening of existing products, and cross-BU synergistic effects
  - Advance patterning solution R&D
  - Integrate technologies (3D NAND development solutions, integrate deposition facilities)
- Strengthen business through strategic investment in focus areas
  - Deposition business: speed up new product development through selection and concentration
  - Cleaning business: enhance products and improve market share by applying best known coater/developers methods

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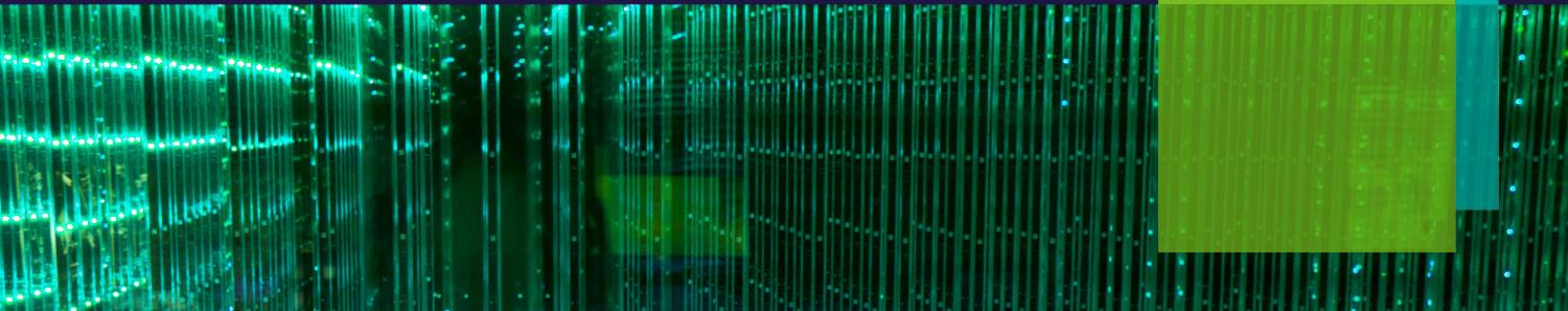
Corporate Development Strategy: Growth Opportunities through Integration

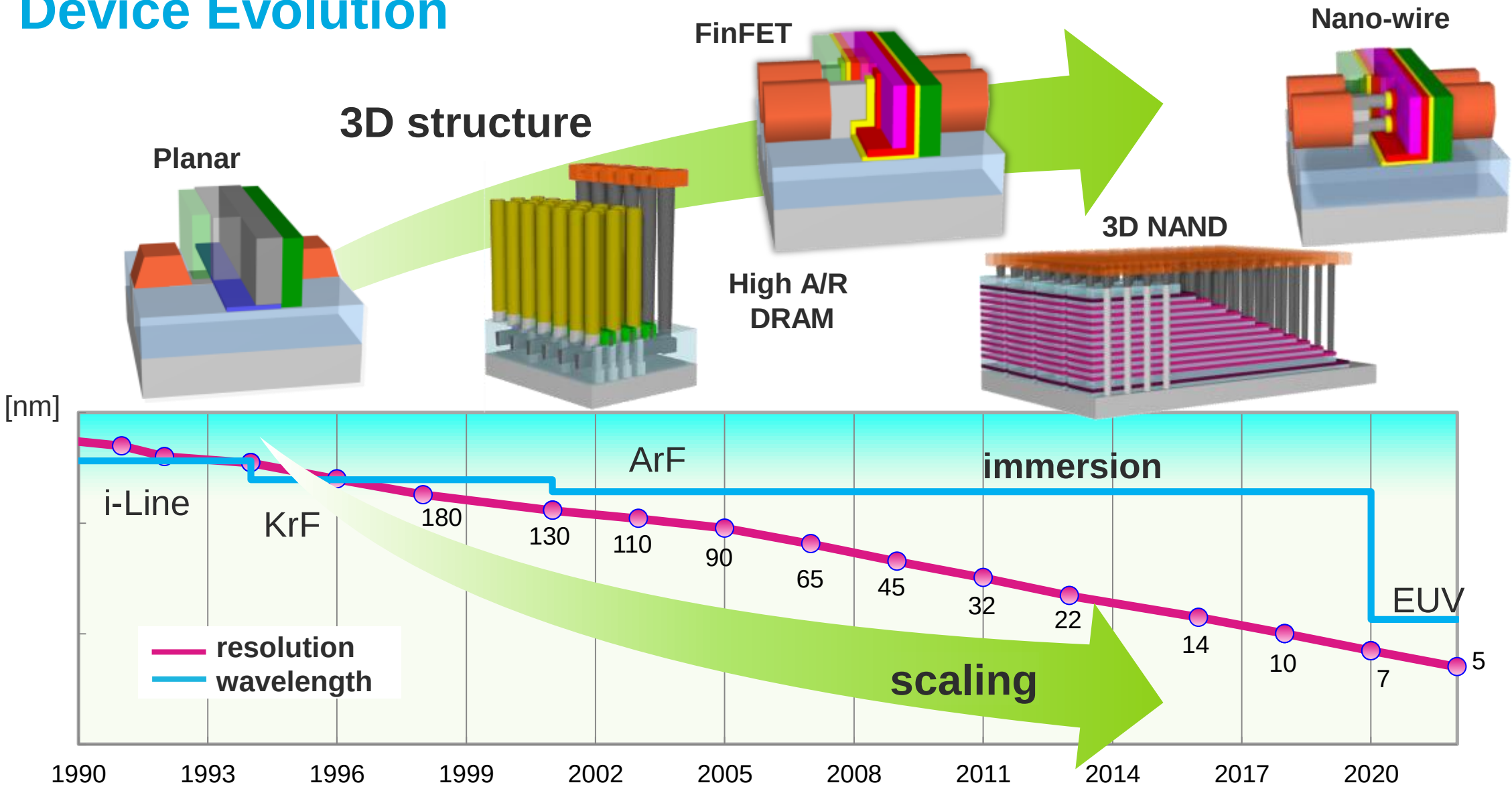
Akihisa Sekiguchi, PhD
Vice President & General Manager
Advanced Semiconductor Technology Division



Contents

- Device roadmap and issues in integration
  - Memory technology roadmap: DRAM, 3D NAND
  - Logic technology roadmap: FEOL, MOL, BEOL
- The importance of Process Integration Center (PIC) within our worldwide R&D

Device Evolution

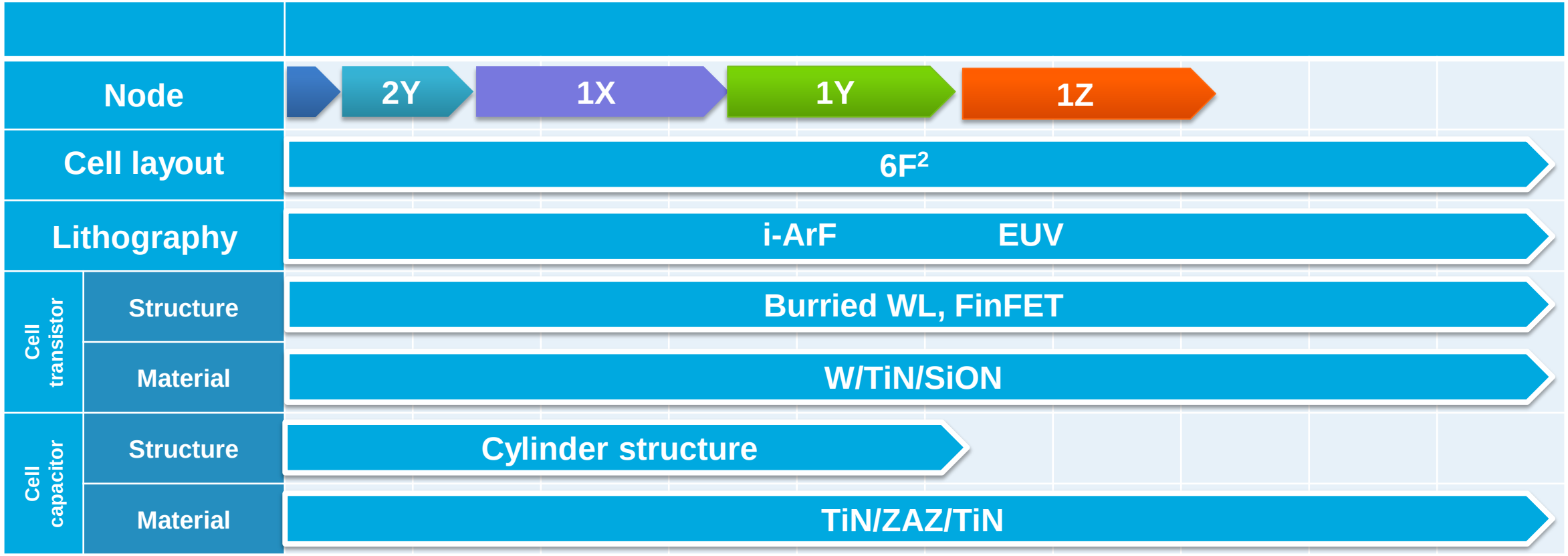


Device Roadmap and Issues in Integration

Memory: **DRAM, 3D NAND**

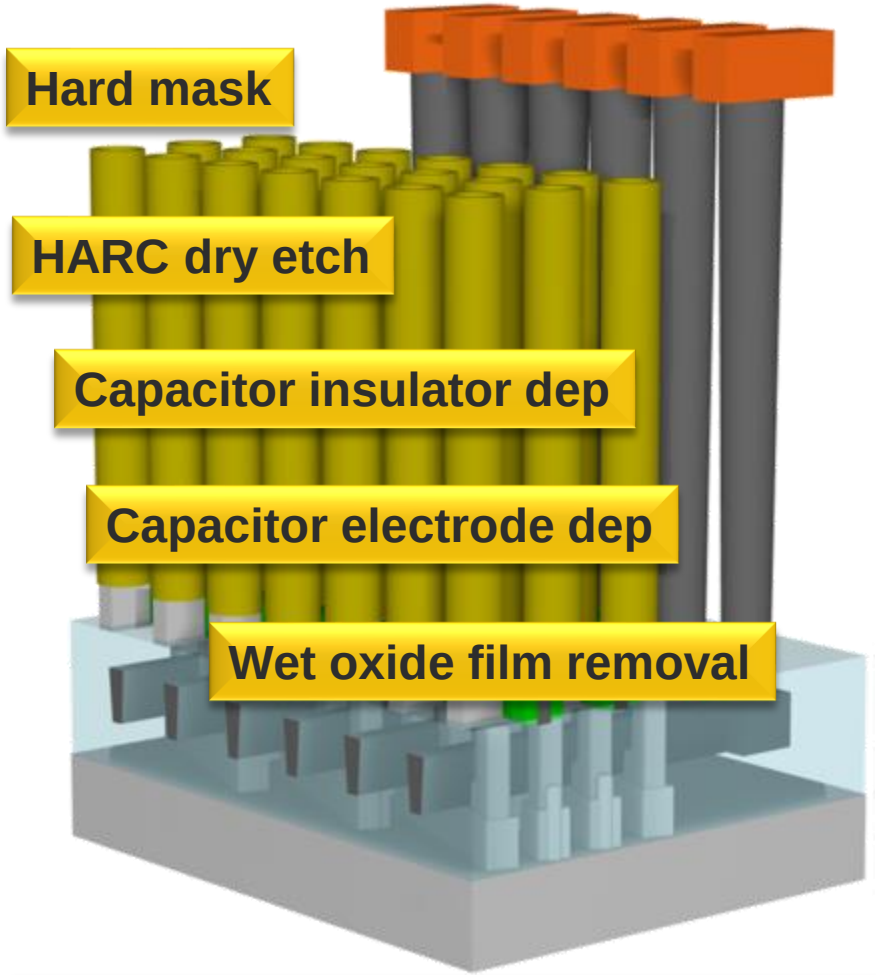
Logic: FEOL, MOL, BEOL

DRAM Roadmap



Difficulty level of scaling has risen beyond 1Y

DRAM Challenge



Dry etching

- ✓ High aspect ratio capacitor (HARC) hole formation
- ✓ High selectivity etch (for insulator etch)

Film deposition

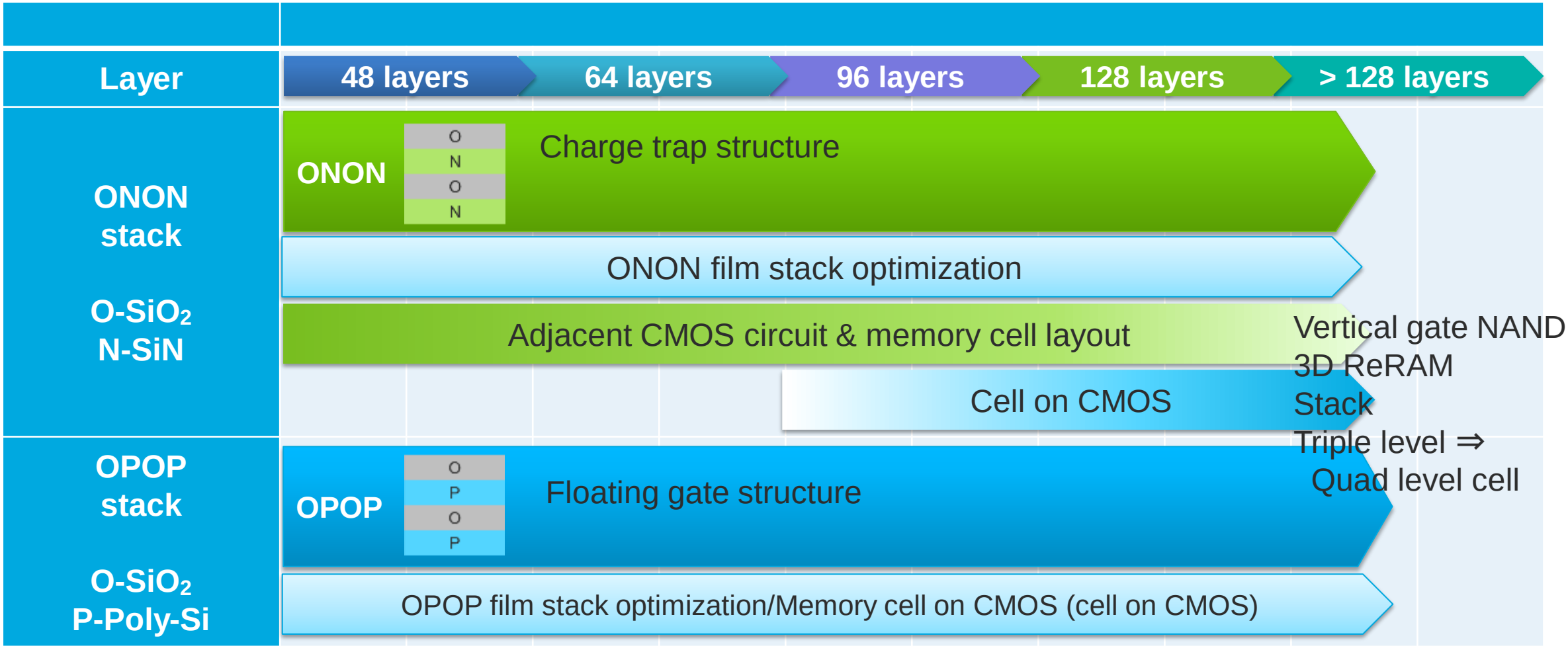
- ✓ High selectivity hard mask (for insulator etch)
- ✓ Conformal & low leakage insulator for capacitor
- ✓ Conformal & low resistance electrode for capacitor

Cleaning/wet etching

- ✓ Prevention of pattern collapse
- ✓ High aspect ratio structure cleaning

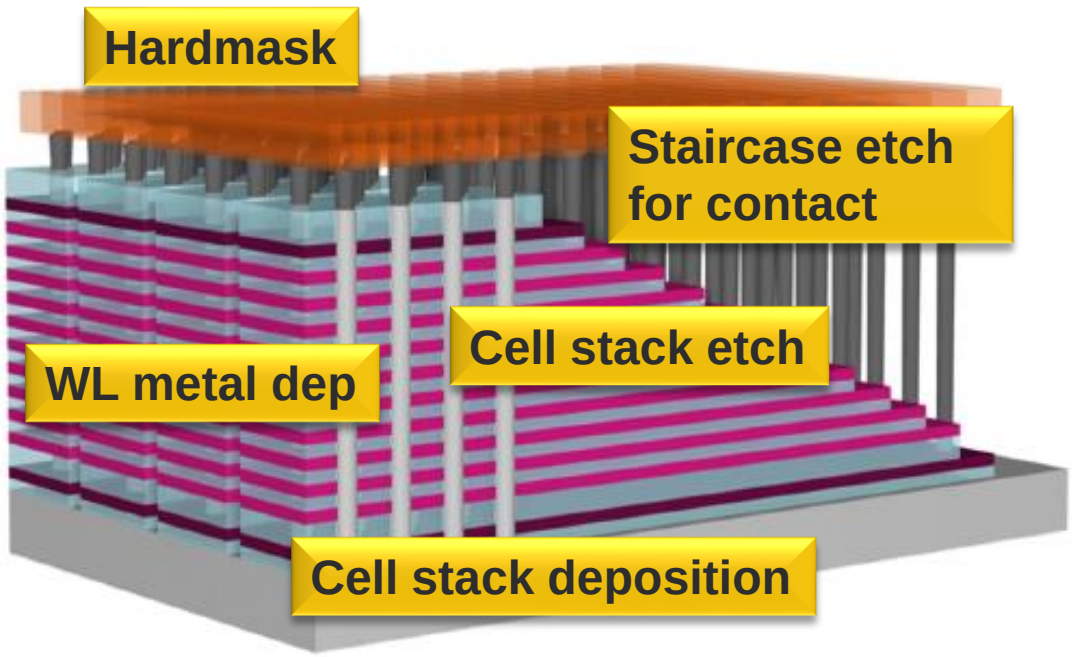
Challenges involving high aspect ratio structures dominate

3D NAND Roadmap



Increasing layers drives high aspect ratio and process challenges

3D NAND Challenges



Dry etch
- ✓ High aspect ratio etch
- ✓ High selectivity (versus stack films)

Depositon
- ✓ Reduction of ONON/OPOP stack warpage
- ✓ High selectivity hardmask
- ✓ Conformal functional film for flash
- ✓ High mobility channel
- ✓ Metal gate

Hardware
- ✓ Handling warped wafers

Clean/wet etch
- ✓ Removal of nitride films in 3D structures

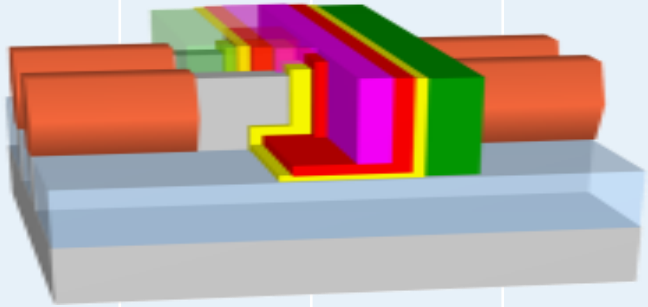
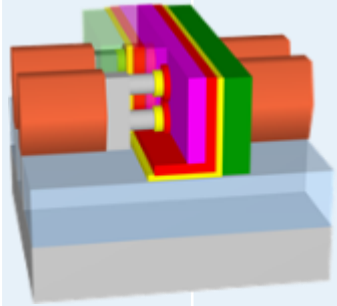
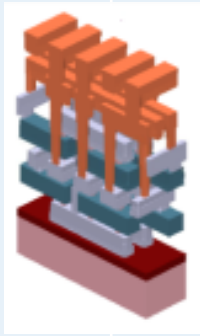
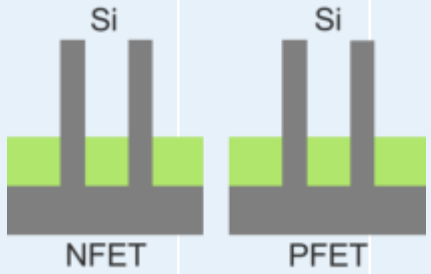
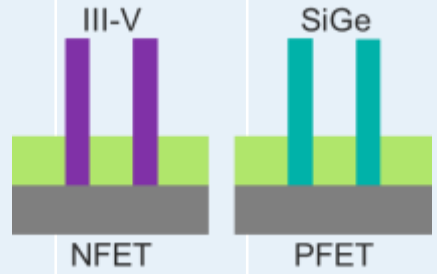
Etch and deposition of films for high aspect ratio structures challenging

Device Roadmap and Issues in Integration

Memory: DRAM, 3D NAND

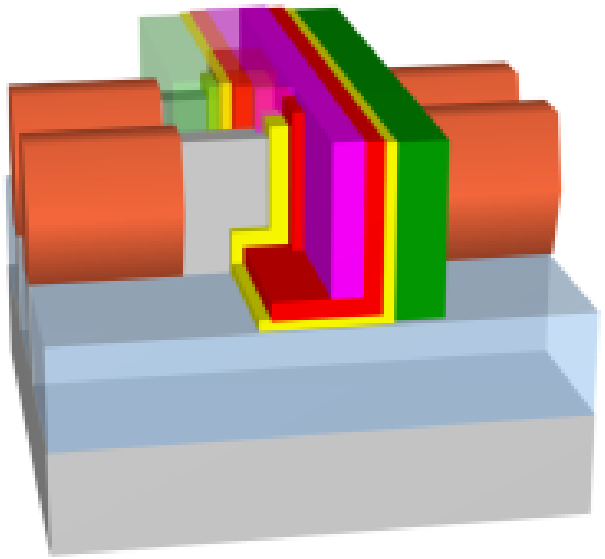
Logic: FEOL, MOL, BEOL

FEOL Roadmap

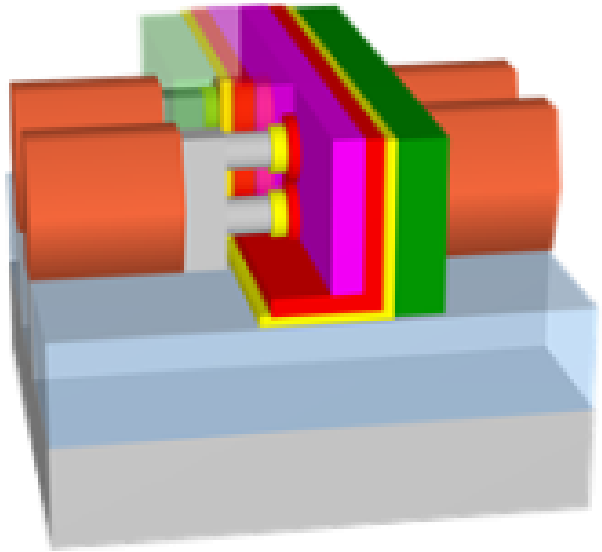
Node	16-14 nm	10 nm	7 nm	5 nm	< 3.5 nm
Transistor structure Reducing short channel effect	 FinFET			 Lateral nanowire	 Vertical nanowire
Channel material Higher mobility					

Structural changes in transistor concurrent with scaling

FEOL Challenges



FinFET

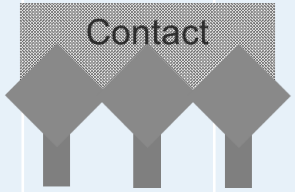
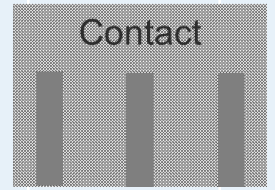
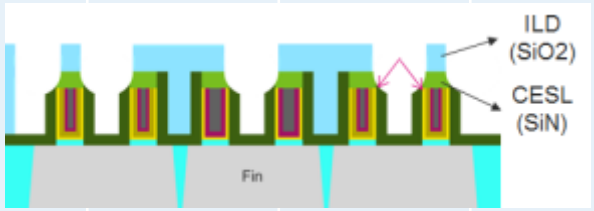
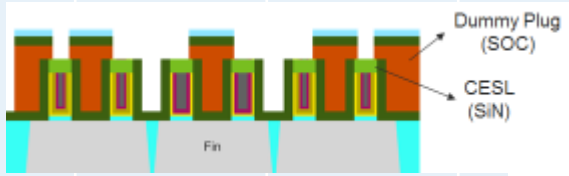
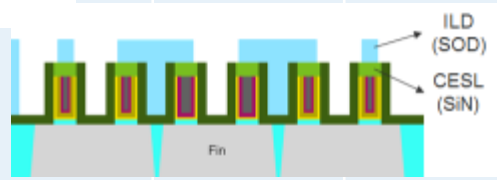
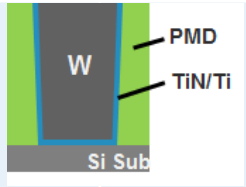
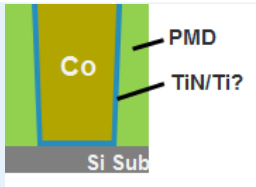


Nanowire transistor

- Short channel effect control (on/off ratio)
  - New structure
- Channel mobility
  - New channel material
- Parasitic resistance reduction
  - Source/Drain activation enhancement
  - Low resistance silicide
- Parasitic capacitance reduction
  - Low dielectric constant material
- Variability reduction
  - Chamber matching, physical dimension control

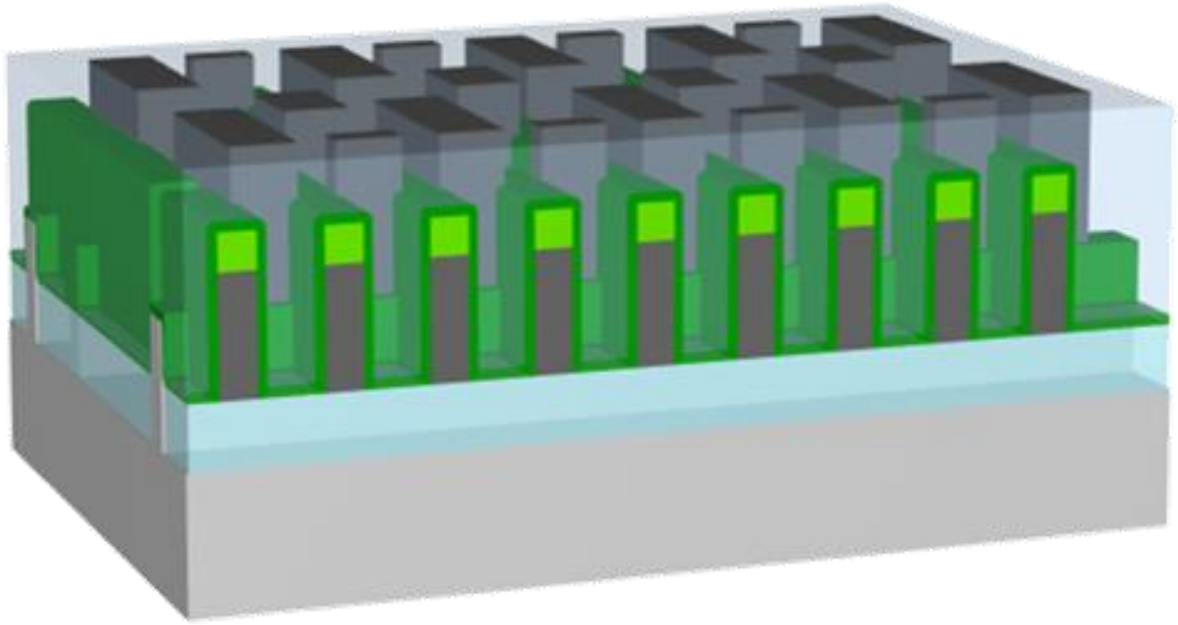
Changes in transistor structure leading to changes in device performance

MOL Roadmap

Node	**16-14 nm**	**10 nm**	**7 nm**	**5 nm**	**< 3.5 nm**
Source/Drain shape	Diamond epi 		Wrap around contact 		
Contact scheme	Self aligned contact 		 Replacement contact 		
Contact metal	 W		 Co		

Scaling, overlay, and contact resistance increase are issues

MOL Challenges

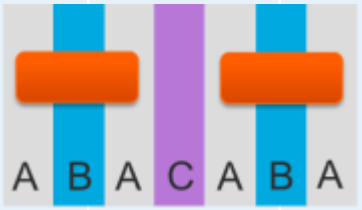
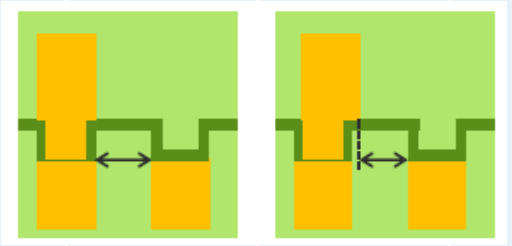
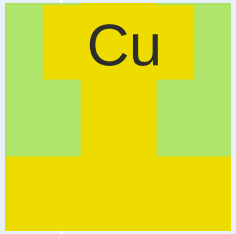


Contact structure

- Parasitic resistance
  - New structure, lower resistance material needed for reduction
- Narrow trench gap fill
  - High aspect ratio structure gapfill
- Overlay
  - Self aligned process
- Variability
  - Chamber matching

Scaling causes problems such as contact resistance increase

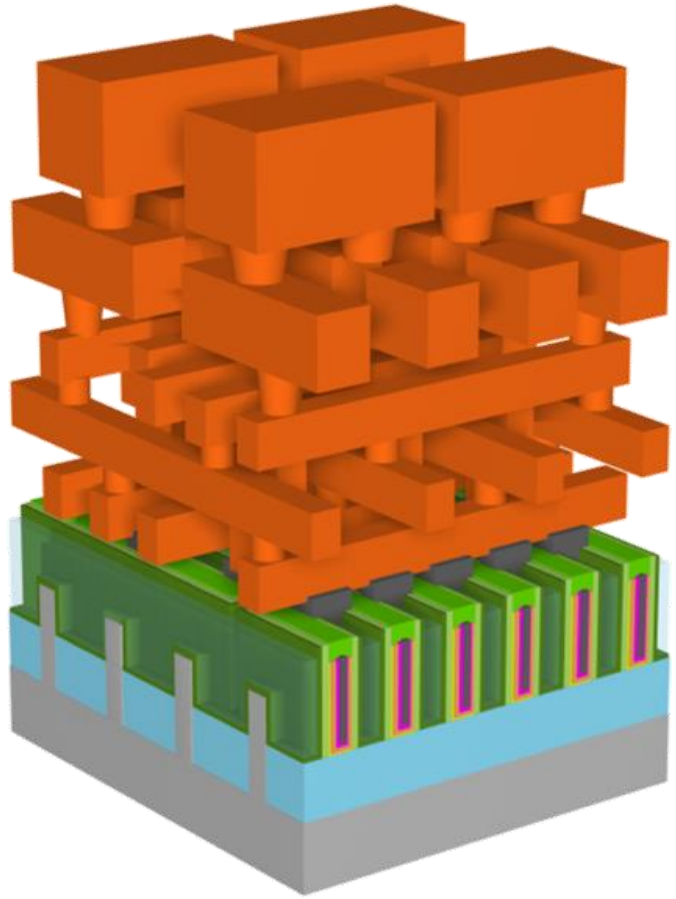
BEOL Roadmap

Node	16-14 nm	10 nm	7 nm	5 nm	< 3.5 nm
Wiring formation scheme	Dual damascene Self aligned via (SAV)  Non SAV SAV		Self aligned block 	Self aligned via formation 	
Metal wiring	Cu : ECD Ta/TaN PVD 		Cu alternatives Ru, Co, CoAl		

Estimated using IEDM, VL, IITC papers

Scaling & overlay issues leading to evaluation of new integration schemes

BEOL Challenges

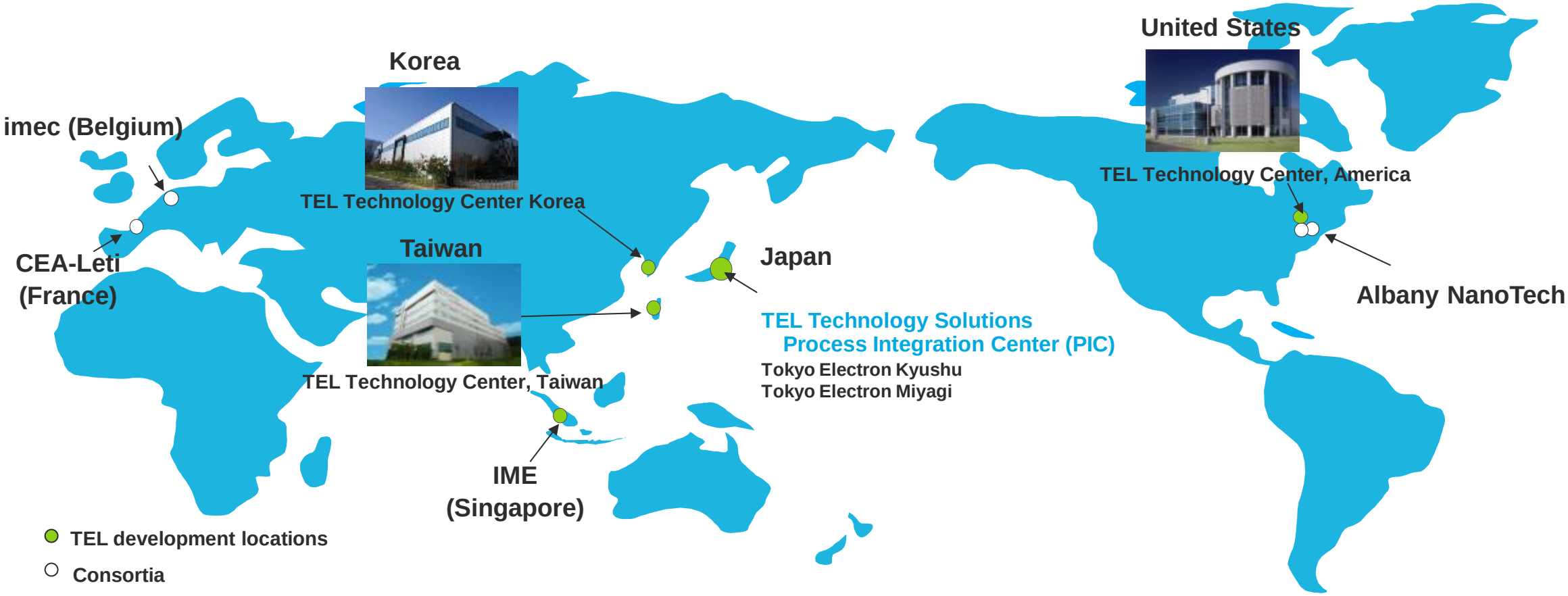


- Low resistance
  - Cu: thinner barrier layer
  - Cu alternatives: Ru, Co, CoAl,
- Parasitic capacitance reduction
  - Low dielectric constant film, air gap
  - Etch damage reduction: low temp etch, replacement schemes
  - Lower dielectric constant etch stop layer
- Narrow trench gap fill
  - Liner layer, alternative metals
- Overlay
  - Self aligned process
- Reliability (migration etc.)
  - Wiring cap layers

Migration period from Cu to other metals, parasitic capacitance still an issue

Importance of Process Integration Center (PIC) in the Context of Worldwide Development

Global Development Locations



Worldwide development accelerated due to strengthening of PIC function

Process Integration Center (PIC) Mission

- Expand business through collaboration with customers
- Add value to TEL products by synchronizing product development and PIC solutions
- Develop competitive solutions in advance in order to make solid proposals based on proven solutions
- Support overall TEL development by making sample wafers with high quality and short lead time, and by providing insights with knowledgeable analysis

Higher level technical collaboration with partners

Process Integration Center (PIC) Function

Process tools

Clean

CELLESTA™ -*i*

Etch

Tactras™ Vigus™

Certas™

Lithography

CLEAN TRACK™
LITHIUS Pro™ Z

Triase+™ / EXIM™

NT333™

TELINDY PLUS™

Deposition

Analytical tools

Analysis and measurement
(Particle, ellipsometer, XRF, overlay)

Cross sectional analysis
(SEM, STEM, FIB, others)

Surface analysis
(TXRF, XPS, XRD, AFM, others)

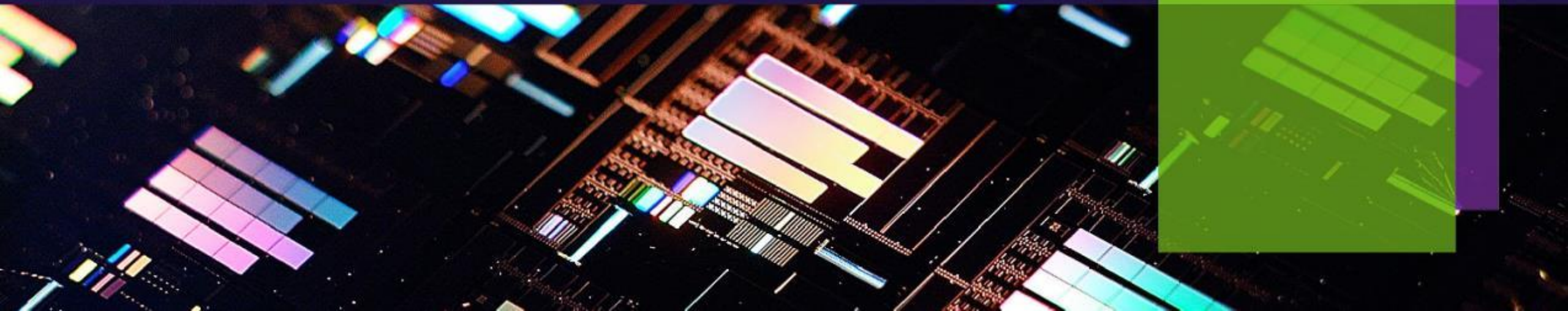
Faster development by centralizing process and analytical tools

Summary

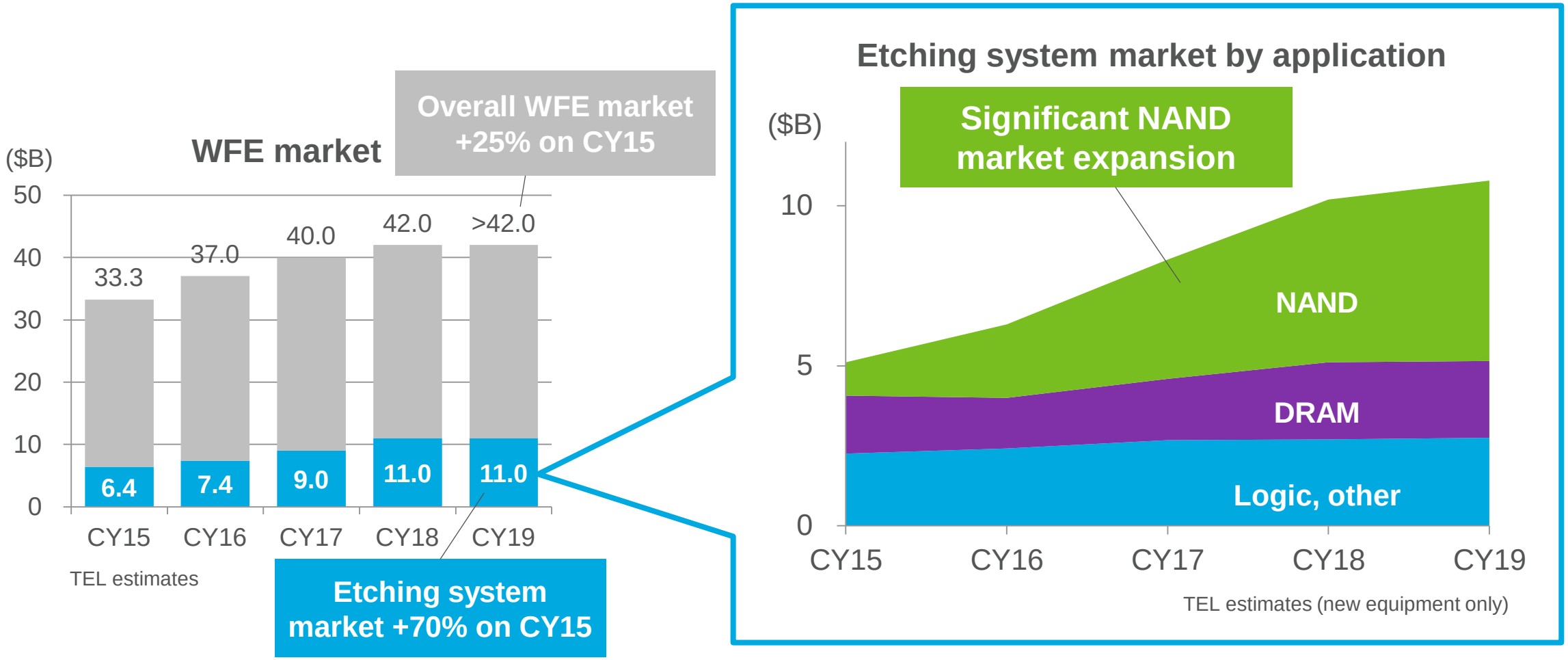
- How to plan ahead and develop new tools based on device evolution is key
- The success of the Patterning Solutions Project has led to the kickoff of Process Integration Center (PIC). It expands on the scope of activities beyond just patterning
- Enhancement of the worldwide development organization by strengthening PIC will lead to TEL's competitiveness
- Continue to create technology innovation through close collaboration with our customers and partners

Etching System: Business Strategies

Yoshinobu Mitano
Vice President & General Manager, ES BU



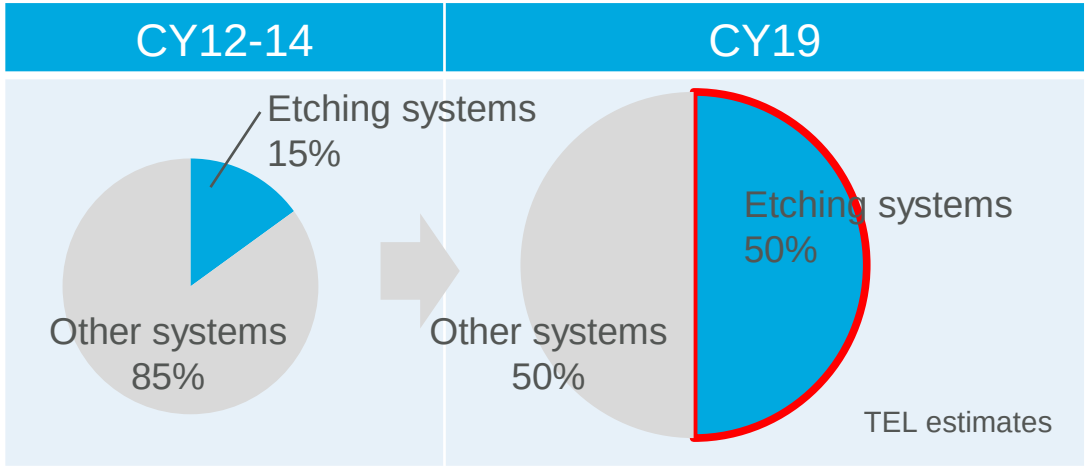
Etching System Market Outlook



3D NAND driving 70% growth in etching system market from CY15 to CY19

3D NAND Business Opportunities

Ratio of etching systems in NAND

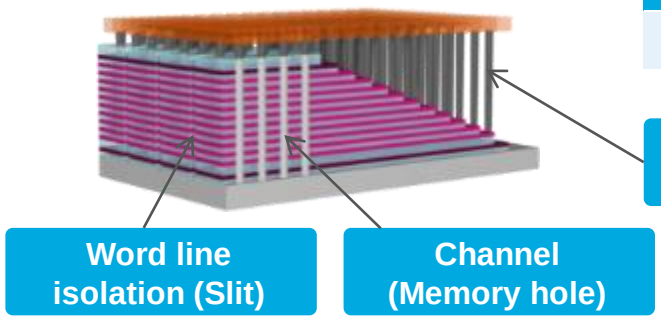


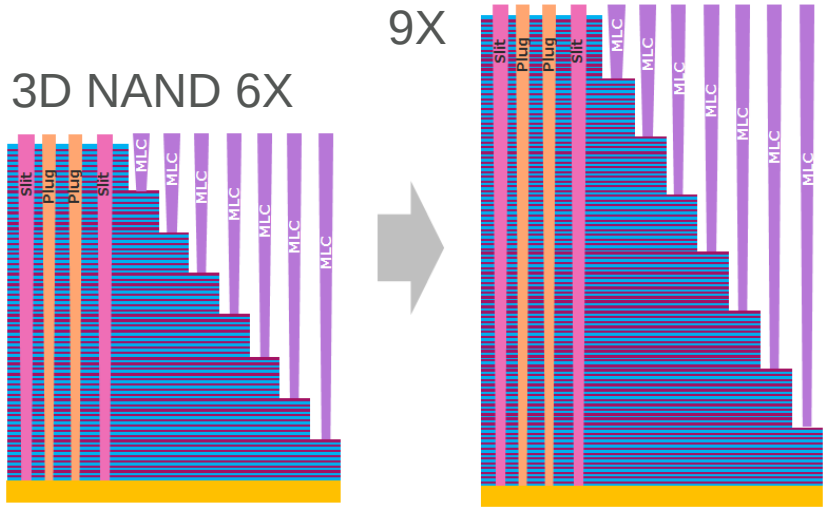
Increase in 3D NAND HARC* processes (Greenfield, TEL estimates)

Investment per 10k/wspm** ($M)	6X	9X	12X
HARC processes (multi-level contact/word line isolation/channel)	30	40	50
Other etching processes	80	80	80
Etching process total	110	120	130

3D NAND HARC* processes

CY17	CY18	CY19
6X	6X/9X	9X





Expand HARC processes by increasing number of stacked layers

* HARC (High aspect ratio contact) process: a process for forming holes that requires advanced processing technology

** wspm: wafer starts per month

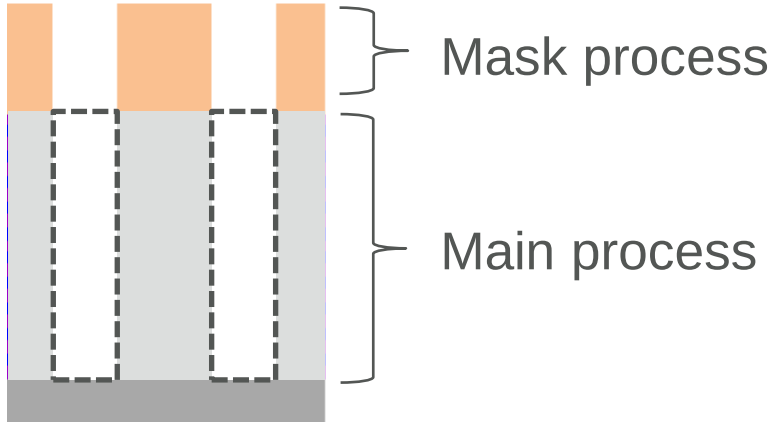
3D NAND: Approach and Results

- Maintained a 100% share of the multi-level contact processes. Plan to further increase revenues by integrating mask process to improve productivity
- Captured new customer PORs with 9X generation word line isolation. Aim to increase our position by integrating mask process
- Realize the capture of channel processes through new technology

Improve productivity by integrating processes

A single system that combines mask and main processes normally processed by different systems

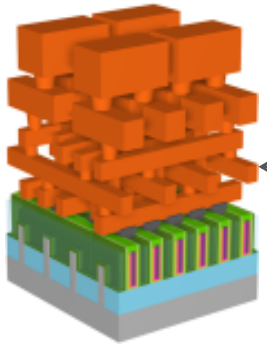
➔ Improved productivity



Expand our position by dramatically improving profile and productivity

Logic: Approach and Results

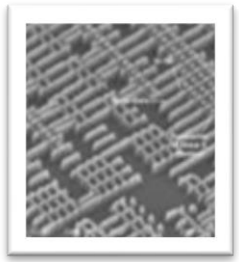
- Maintained high interconnecting dielectric etching process market share
- Aim to expanded advanced patterning applications



Interconnects
Advanced patterning

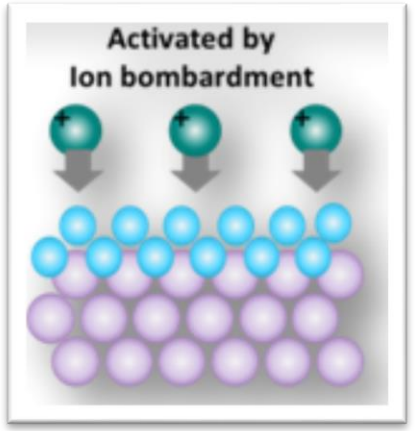
RLSA™ plasma source

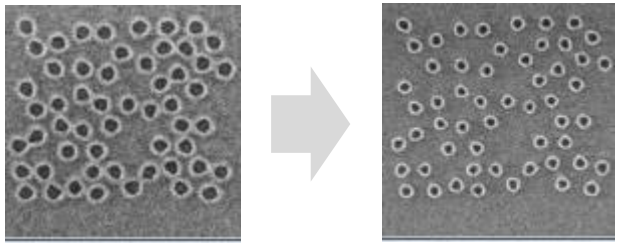
Plasma etch systems
Tactras™ RLSA™



Realize high selectivity through low electron temperature plasma

ALE concept process



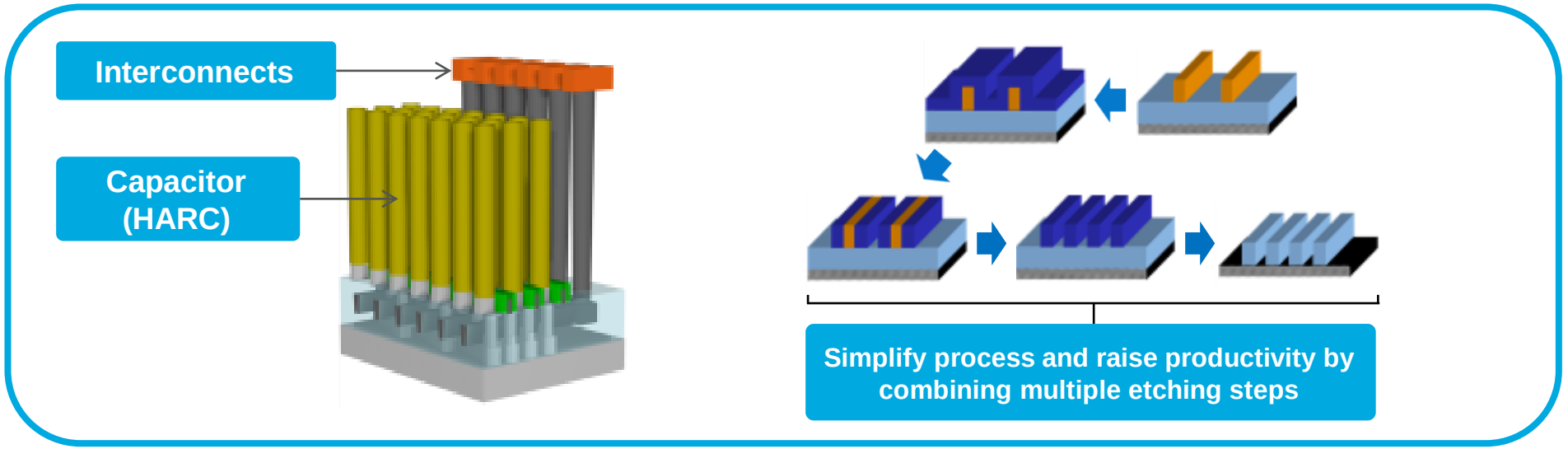


Achieve high-level of control over dimension variation

Aim to increase sales by differentiating our technology in 7nm and finer advanced patterning

DRAM: Approach and Results

- Captured BEOL processes by leveraging expertise in logic through our strength in damascene processes
- Captured development PORs with all customers using 1Y generation capacitor process (HARC)
- Realized reduced patterning costs for customers by combining etching steps.
  Currently using successes with strategic customers to expand market share in other customers



Currently achieving success in all DRAM focus processes in line with plan

Action to Increase Profitability

- New products focused on the high-end market
  - ➔ Active capex in R&D
- Reduce customer support expenses through products with improved added-value
- Optimize logistics
- Further reduce fixed cost ratio

Tokyo Electron Miyagi's new development and logistics buildings

Plan to raise sales and profits through technological differentiation and improving production efficiency

Summary

- Expect significant expansion of etching system market driven by 3D NAND and patterning
- We are enhancing our positions in logic and memory focus areas
- Actively investing in R&D in response to further market expansion
- Focus on HARC, patterning, and BEOL processes that utilize our strengths. Aim to raise profitability by increasing market share to over 30% by CY19

Market share	CY14 (Actual)	CY15 (Actual)	CY16 (Actual)	・・・	CY19 (Target)
Etching system	28%	21%	23%		>30%

TOKYO ELECTRON

FPD Business Strategy

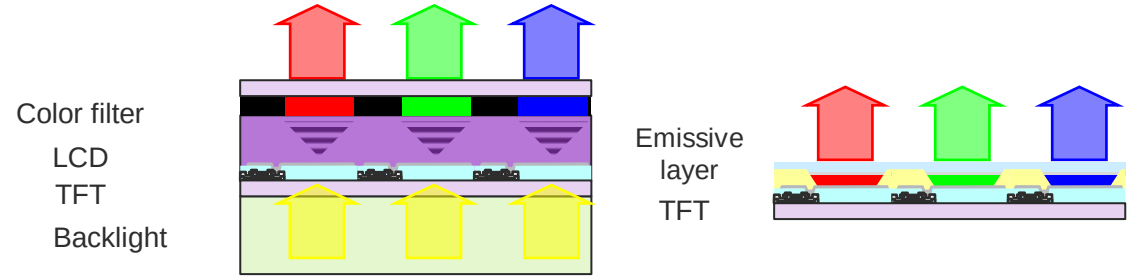
Tsuguhiko Matsuura
Vice President & General Manager, FPD BU

Display Trends

Technology inflection creates greater business opportunities

Increasing screen size

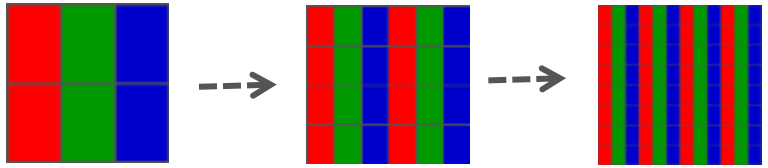
OLED



LCD ------> OLED

Increasing resolution

TV



FHD --> 4K --> 8K

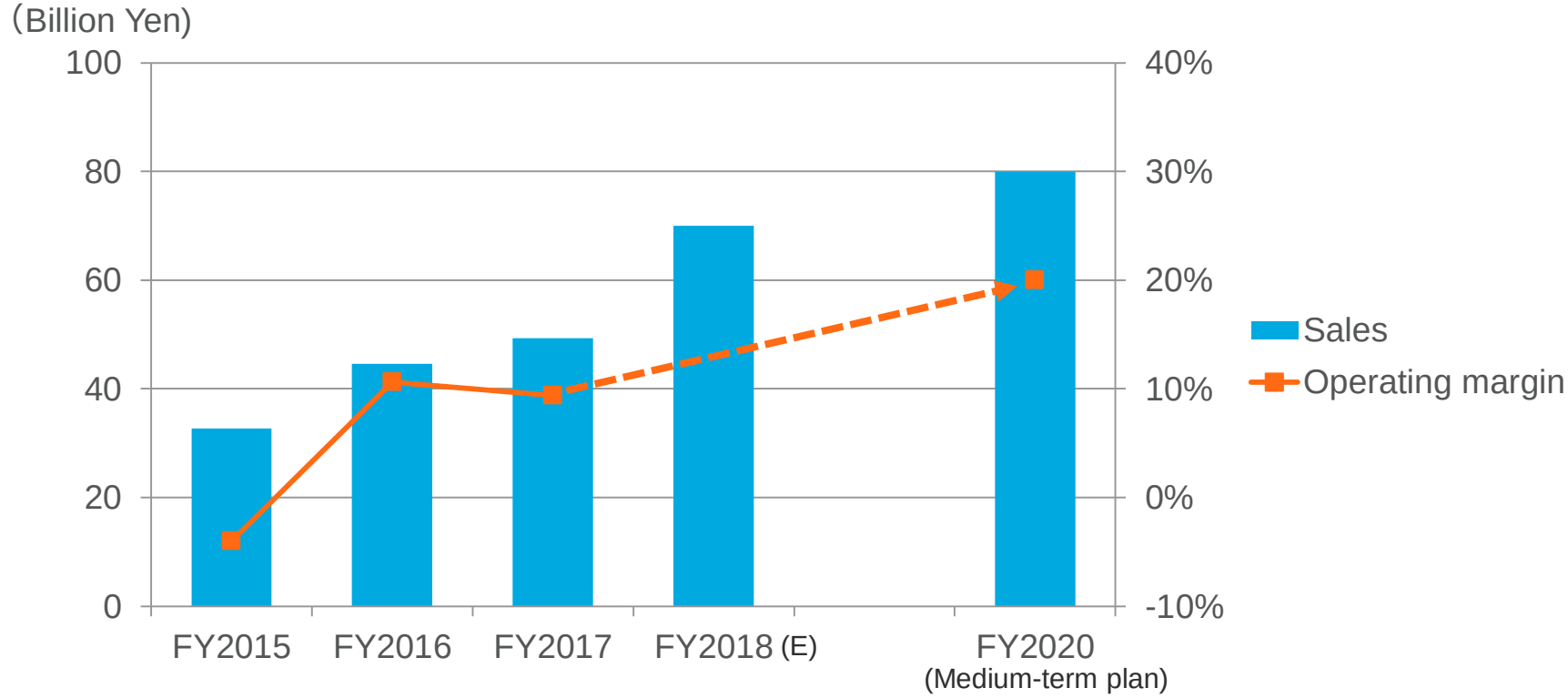
Smartphones 300 ppi -----> 700 ppi

Design flexibility

Flexible, edge bent, free format

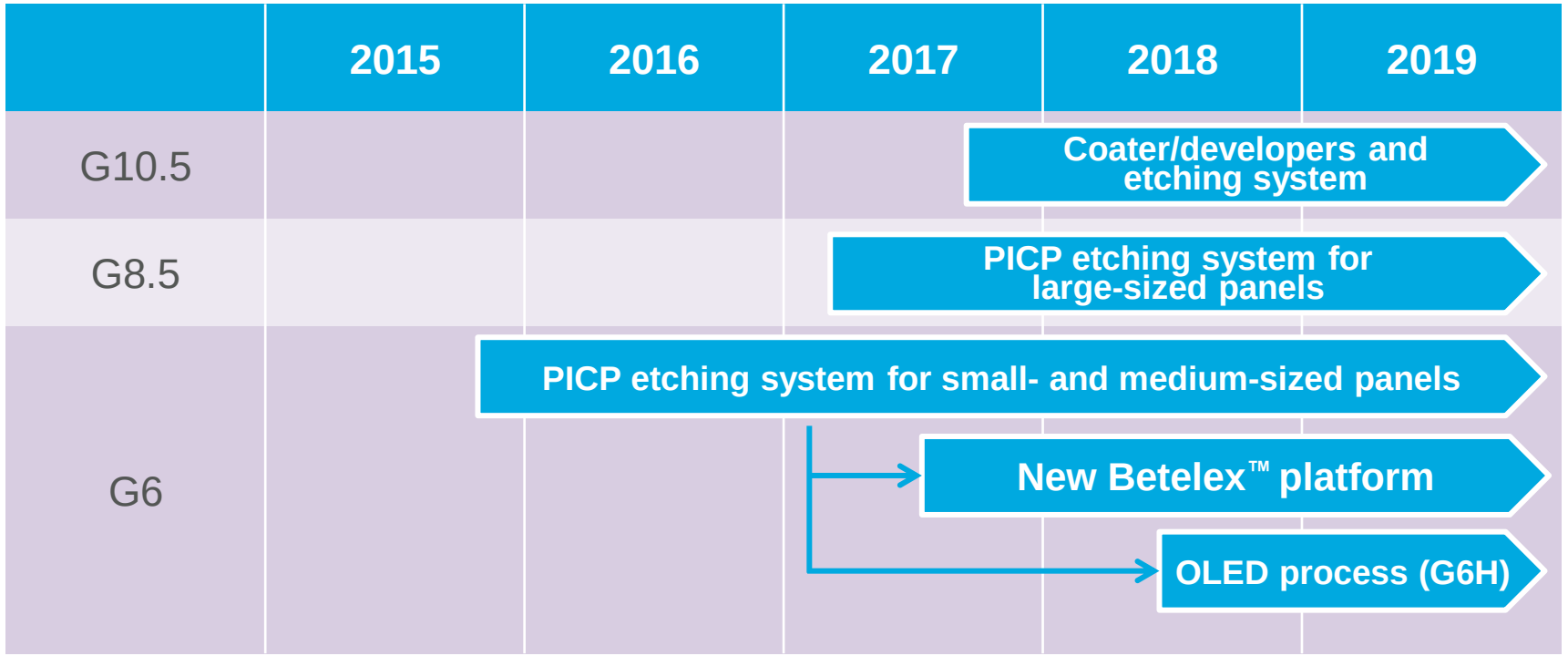
FPD Business Medium-term Plan

- Increase share and profitability in market that has begun to grow again
- FY2020 target: sales ¥80.0B, operating margin over 20%



Medium-term Plan Progress: Highlights

- TEL's product strategy for a new PICP™* etching system is progressing according to plan
- Expanding the G10.5 equipment business



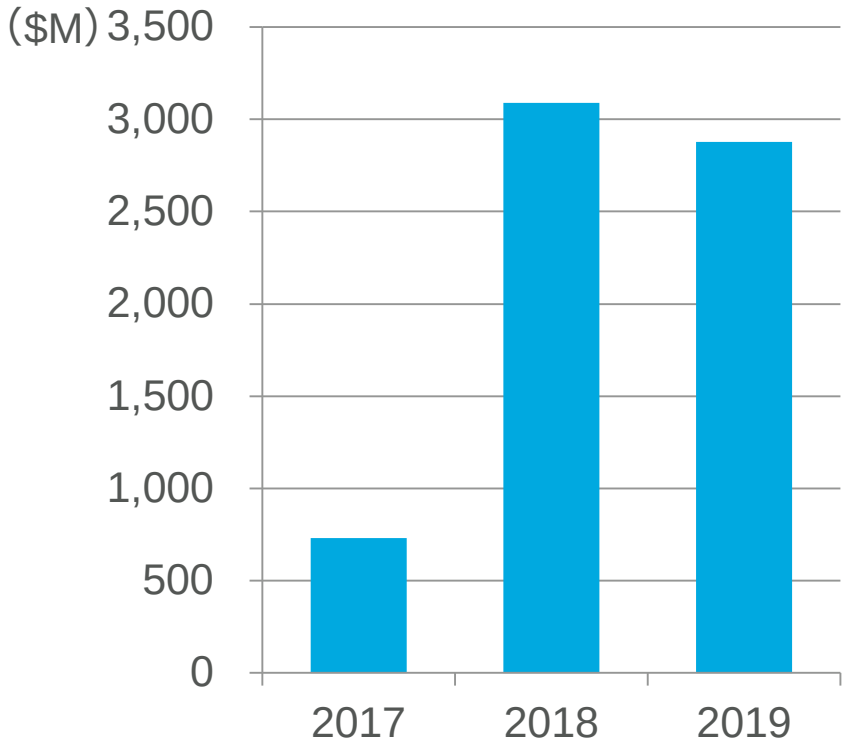
Higher profitability for all panel generations

* PICP: Plasma source for producing extremely uniform high density plasma on substrate

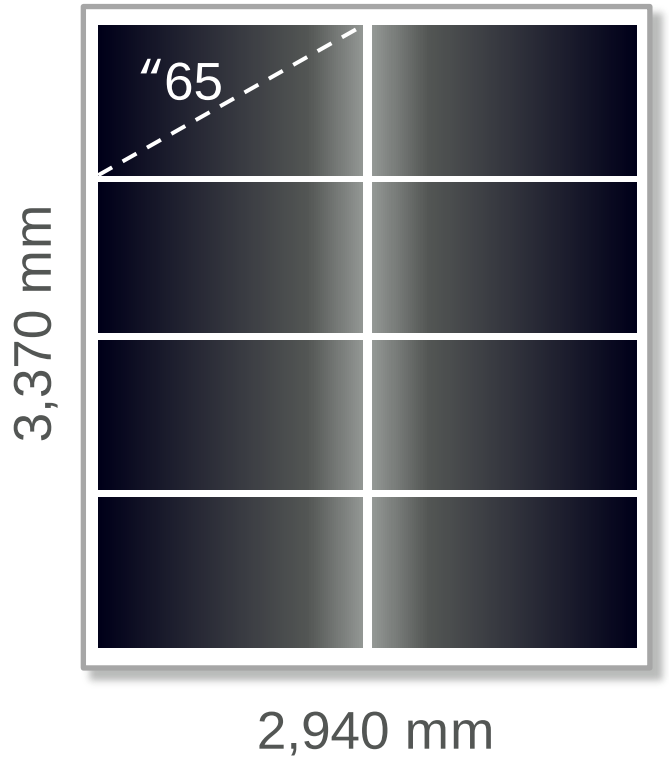
Opportunity – G10.5 Equipment Market

- Greater than expected investment and market expansion
- Maintain high market share through technological differentiation (large area plasma suppression, air floating coater)

G10.5 TFT array equipment market



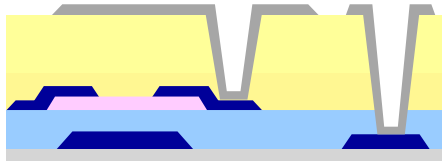
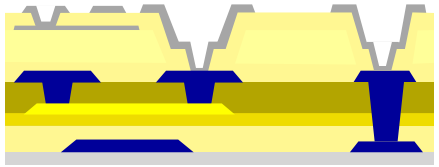
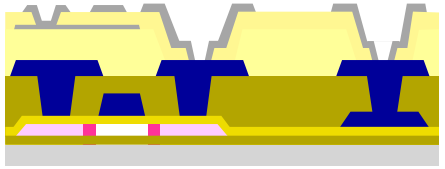
Eight 65 inch TV panel substrate possible



Results based on IHS Markit, Technology Group "Display Supply Demand & Equipment Tracker, Q1 2017". Results are not an endorsement of Tokyo Electron. Any reliance on these results is at the third party's own risk. Visit technology.ihs.com for more details.

Opportunity – Metal Oxide/LTPS

- Higher sophistication of etching technology and increased number of processes

TFT	a-Si	Metal oxide	LTPS
Representation of structure			
Application	LCD TV Monitor	OLED TV Tablet	Smartphone (LCD/OLED)
Number of masks	5	6 - 8	9 - 13
Dry etch processes	3 a-Si, SiNx	3 SiO, SiNx	-11 SiO, Metal

Further new needs

Flexible displays
＋2 processes

OLED process
(G6 half size)
＋3-4 processes

Opportunity – Growth of OLED TV Market

- Introduced inkjet printing system to meet production demand from 2018
- Material utilization significantly more efficient than current evaporation method

Increase in OLED TV manufacturers

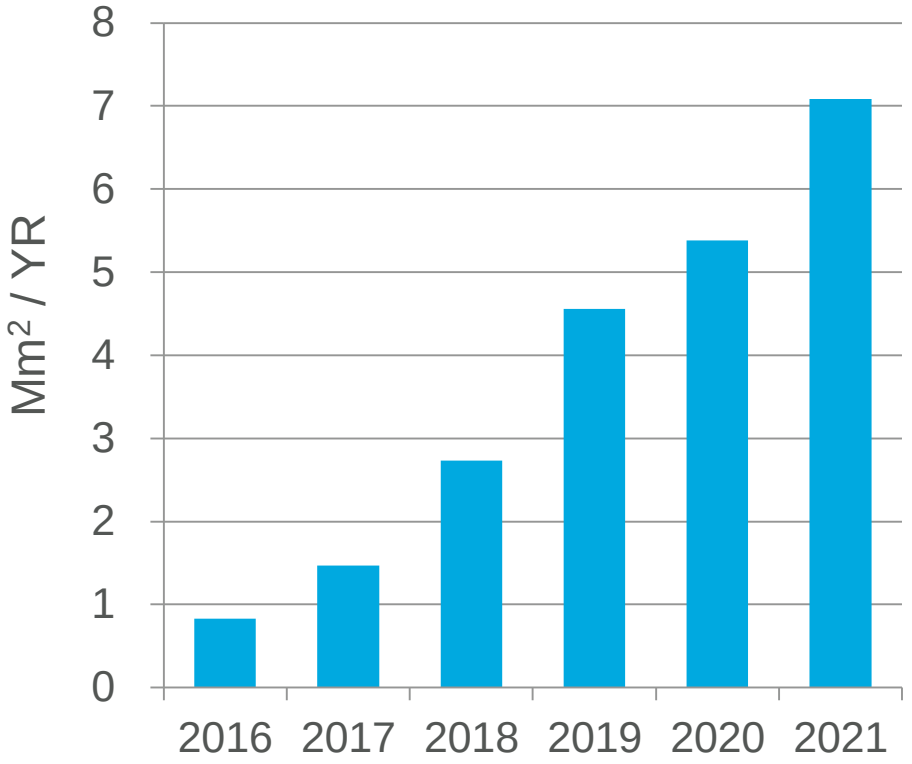
New manufacturers in Japan

Toshiba
- REGZA X910 series
- Launched March 2017

Sony
- BRAVIA A1
- To be launched June 2017

Panasonic
- VIERA TH-65EZ1000/EZ950 series
- To be launched June 2017

OLED TV area demand



Results based on IHS Markit, Technology Group “Display Supply Demand & Equipment Tracker, Q1 2017”. Results are not an endorsement of Tokyo Electron. Any reliance on these results is at the third party's own risk. Visit technology.ihs.com for more details.

Summary

- Increase share and profitability in market that has begun to grow again

  Greater than expected business expansion

  FY2020 target: sales ¥80.0B, operating margin over 20%

- For leading-edge production process, focus on areas where we have technological superiority

  – High performance PICP etching system

  – G10.5 compatible etching system and coater/developers

  – Inkjet printing system for OLED TV

Financial Model

Tetsuro Hori
Representative Director, Executive Vice President & General Manager

Financial Model: Concept

- TEL is changing its financial model to match the larger scale of the semiconductor market
- Financial model: Change in WFE* market scale
  - In our financial model announced in 2015 we presented a range according to economic conditions (WFE $37B-$30B)

    (Equipment for wafer-level packaging is not included)
  - Our new financial model presents a forecast range for FY2020. We expect the WFE market to reach a size of $42B to $45B

    (Equipment for wafer-level packaging is included)

* WFE (Wafer Fab Equipment): The semiconductor production process can be divided into two sequential sub-processes: front-end (wafer fabrication) and back-end (assembly and test) production. WFE is used in the front-end production process.

Financial Model (toward FY2020)

(Billion Yen)

	FY2017 (Actual)	FY2018 (Estimate)	FY2020 (Medium-term plan)	
	WFE $37B	WFE $40B	WFE $42B	WFE $45B
Net sales	799.7	980.0	1,050.0	1,200.0
SPE	749.8	910.0	970.0	1,120.0
FPD	49.3	70.0	80.0	80.0
Gross profit	322.2	412.0	452.0	522.0
Gross profit margin	40.3%	42.0%	43.0%	43.5%
SG&A expenses	166.5	196.0	200.0	210.0
SG&A expense ratio	20.8%	20.0%	19.0%	17.5%
Operating income	155.6	216.0	252.0	312.0
Operating margin	19.5%	22.0%	24.0%	26.0%
Net income attributable to owners of parent	115.2	163.0	180.0	220.0

SPE Sales (WFE $45B)

➢ TEL continues to plan for growth in sales above market growth

(Billion Yen)

	FY2017 (Actual)	FY2018 (Estimate)	FY2020 (Medium-term plan)	Growth (FY17-FY20)
	WFE $37B	WFE $40B	WFE $45B	WFE +22%
Sales	749.8	910.0	1,120.0	+49%
New equipment	550.3	660.0	810.0	+47%
Field solutions	199.4	250.0	310.0	+55%

- Differentiate our technology in products and continue to win PORs
- Meet expanding demand for field solutions

FPD Sales

- Plan to expand sales based on differentiated technology and high-market-share products

(Billion Yen)

	FY2017 (Actual)	FY2018 (Estimate)	FY2020 (Medium-term plan)	Growth (FY17-FY20)
Sales	49.3	70.0	80.0	+62%
New equipment	40.5	60.0	70.0	+73%
Field solutions	8.8	10.0	10.0	+13%

- In OLED panels where high level technology is in demand, differentiate with cutting-edge PICP™* technology
- Further expand sales for G10.5, where TEL has a high market share
- Continue development of inkjet printing system for OLED TVs

* PICP: Plasma source for producing extremely uniform high density plasma on substrate

Gross Profit (WFE $45B)

➢ Gross profit margin: up 3.2pts

(Billion Yen)

	FY2017 (Actual)	FY2018 (Estimate)	FY2020 (Medium-term plan)	Growth (FY17-FY20)
Gross profit	322.2	412.0	522.0	+62%
Gross profit margin	40.3%	42.0%	43.5%	+3.2pts

- Raise marginal profit ratio of core SPE products
  - Timely introduction of new products to an expanding market
  - Lower cost ratio through product quality improvements
- Raise marginal profit ratio of FPD production equipment

SG&A Expenses (WFE $45B)

➢ SG&A expense ratio: improve by 3.3pts

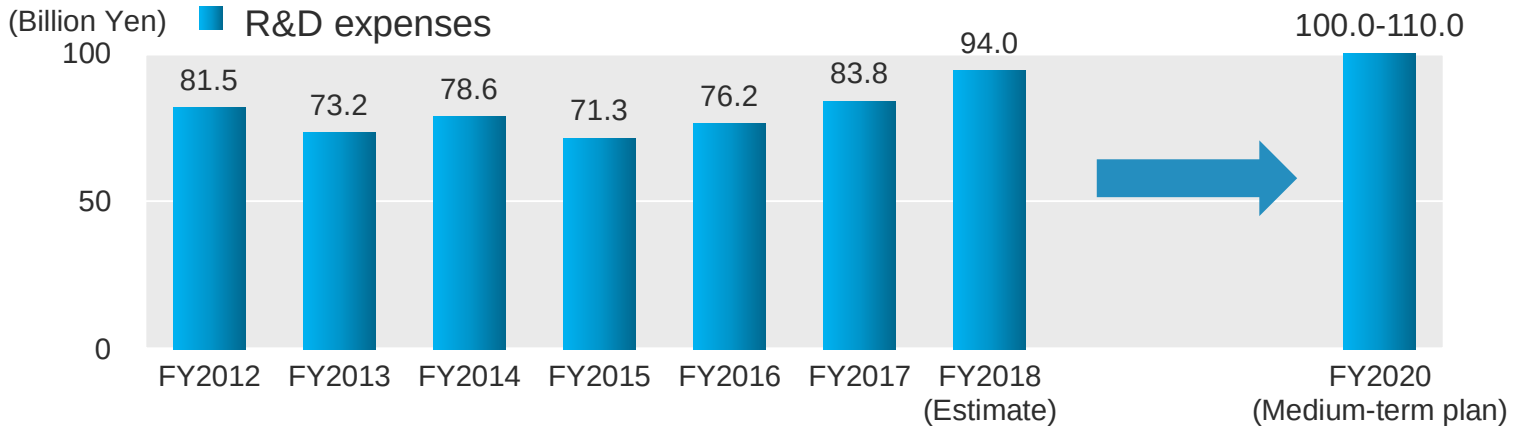
(Billion Yen)

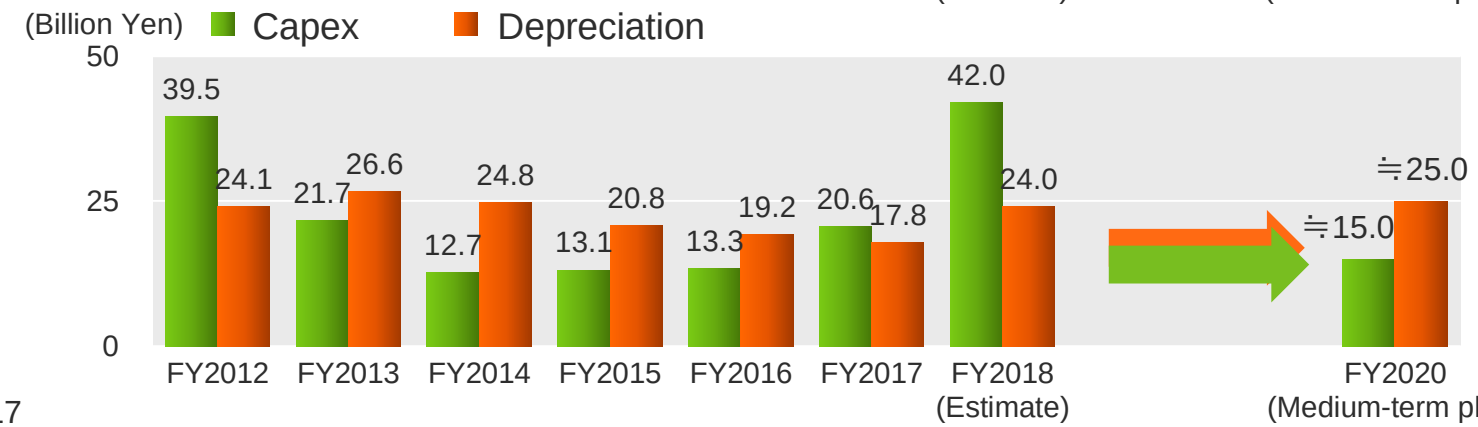
	FY2017 (Actual)	FY2018 (Estimate)	FY2020 (Medium-term plan)	Growth (FY17-FY20)
SG&A expenses	166.5	196.0	210.0	+26%
SG&A expense ratio	20.8%	20.0%	17.5%	-3.3pts

- Cost reductions through integration of development units
  - Establish Tokyo Electron Technology Solutions Ltd.
  - Realized benefits of integration of Coater/Developers and Cleaning System business units
- Raise business productivity, control fixed costs
  - Improve business efficiency of service divisions
  - Control development expenses at level appropriate to balance with current profitability

R&D Expenses, Capex Plans

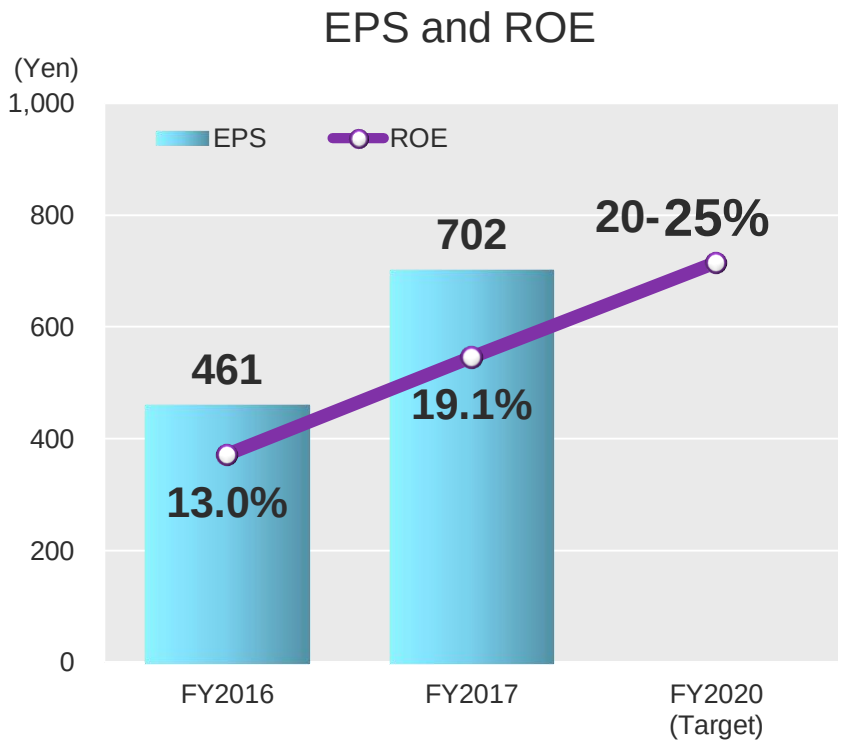
- Implement product development needed for growth, while raising efficiency and maintaining profits
- Capex (development + production facilities) to be limited to around ¥15.0B annually





Assets and Capital Efficiency (Sales ¥1,200B Model)

- Accounts receivable turnover
  – Current approx. 60 days: Appropriate
- Inventory turnover
  – Current 108 days → Target 95 days
- ROE
  – Current 19% → Target 20-25%



ROE = (Net income attributable to owners of parent / Average total equity) x 100(%)

Medium-term Financial Targets (toward FY2020)

Aim for sustained growth in corporate value and continue to develop next-generation products while maintaining a global standard level of profitability

WFE* Market size	$42B	$45B
Net sales	¥1,050B	¥1,200B
Operating margin	24%	26%
ROE (Return on Equity)	20-25%	

- WFE (Wafer fab equipment): The semiconductor production process can be divided into two sequential sub-processes: front-end (wafer fabrication) and back-end (assembly and test) production. WFE is used in the front-end production process. Front-end production equipment includes equipment for wafer-level packaging.

Capital Policy, Shareholder Returns

- Approach to capital policy
  - While closely monitoring the business environment and our necessary cash balance, we will strive to raise ROE through earnings maximization and asset turnover improvement to efficiently utilize shareholders equity
- Approach to shareholder policy
  - Business trends in our industry can be volatile and our policy is to link dividend payments to business performance
  - However, to assure stable returns to our shareholders, we will utilize our sound financial foundation to establish a minimum DPS payment

Dividend payout ratio: 50%

Annual DPS of not less than ¥150

We will review our policy if the company does not generate net income for 2 consecutive fiscal years

We will flexibly consider share buybacks

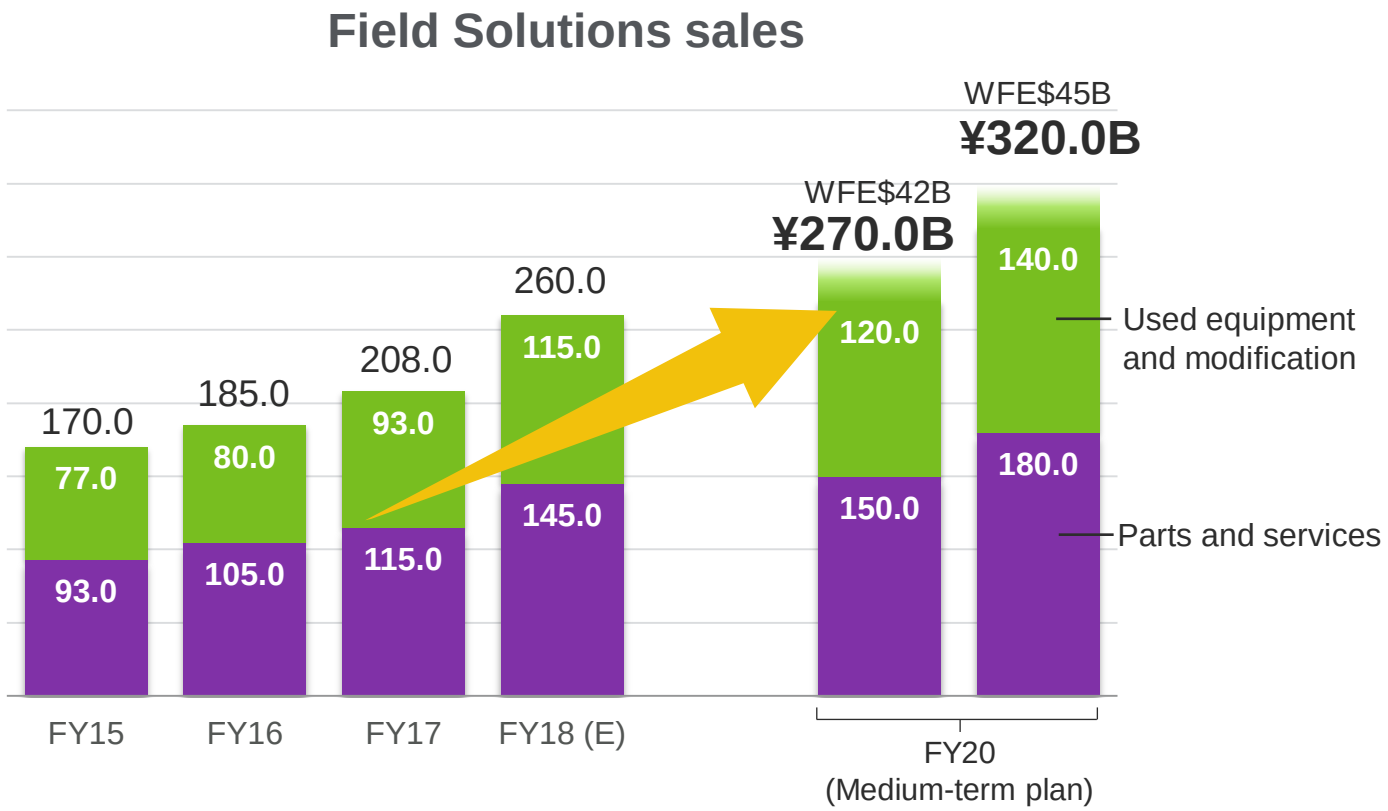
Summary

- Steadily work to achieve our FY2020 financial model
- Further strengthen product competitiveness, aim for sales growth greater than market growth
- Raise development efficiency and business productivity, further improve profitability

Pursue a global standard level of profitability, aim for sustained growth in corporate value

Appendix

Field Solutions (FS) Business: Medium-term Plan



FS business strategy

- Respond to new customer needs driven by IoT
  - Provide upgrades and remanufactured equipment that handle new applications
- Contribute to improving customer productivity
  - Provide added-value services using remote connections

(Installed base of 62,000 units)

Increase earnings in both the used equipment/modification and parts/service segments through a business model that utilizes makers' strengths

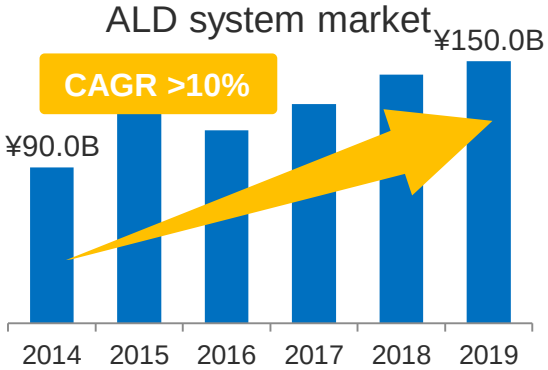
SPE Business Strategy: Deposition System

Aim to expand earnings based on new technologies for further miniaturization and next-generation semiconductors

ALD system

- Achieve both high quality film formation and high productivity needed for miniaturization and for 3D structure with semi-batch system

Semi-batch ALD system
NT333™



Source: TEL estimate

CVD system

- Differentiate in memory through our clear lead in batch system productivity
- Achieve high quality metallization to enable further miniaturization

Batch system
TELINDY PLUS™

Metallization system
Triase+™

Market share	CY14 (Actual)	CY15 (Actual)	CY16 (Actual)	・・・	CY19 (Target)
Deposition system	38%	38%	37%		>47%

Source: Gartner, "Market Share: Semiconductor Wafer Fab Equipment, Worldwide, 2016", 30 March 2017, Charts/graphics created by Tokyo Electron based on Gartner research.
Deposition System: Tube CVD + Atomic layer deposition tools + Oxidation/diffusion furnaces + Nontube LPCVD

Adjustment to Share Results due to Product Recategorization
(etching system, cleaning system)

- From CY2016 dry cleaning systems have been recategorized under etching system, and actual shares for etching system and cleaning system for CY2014, CY2015 and CY2016 have been adjusted to reflect this

Before adjustment

Market share	CY2014	CY2015	CY2016
Etching system	26%	19%	21%
Cleaning system (Including dry cleaning systems)	24%	23%	25%

After adjustment

Market share	CY2014	CY2015	CY2016
Etching system (Including dry cleaning systems)	28%	21%	23%
Cleaning system	19%	18%	20%

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  Forecast of TEL's performance and future prospects and other sort of information published are made based on information available at the time of publication. Actual performance and results may differ significantly from the forecast described here due to changes in various external and internal factors, including the economic situation, semiconductor/FPD market conditions, intensification of sales competition, safety and product quality management, and intellectual property-related risks.

- Processing of numbers
  For the amount listed, because fractions are rounded down, there may be the cases where the total for certain account titles does not correspond to the sum of the respective figures for account titles. Percentages are calculated using full amounts, before rounding.

- Exchange risk
  In principle, export sales of Tokyo Electron's mainstay semiconductor and FPD panel production equipment are denominated in yen. While some settlements are denominated in dollars, exchange risk is hedged as forward exchange contracts are made individually at the time of booking. Accordingly, the effect of exchange rates on profits is negligible.

- Disclaimer regarding IHS Markit data (Page 63, 65)

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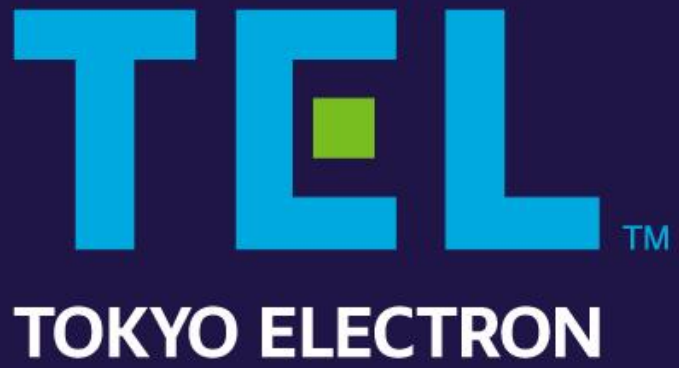
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